A Platform for Analyzing DDR3 and DDR4 DRAMs

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***Abstract*—The authors explore the intrinsic trade-off in a DRAM between the power consumption (due to refresh) and the reliability. Their unique measurement platform allows tailoring to the design constraints depending on whether power consumption, performance or reliability has the highest design priority. Furthermore, the authors show how this measurement platform can be used for reverse engineering the internal structure of DRAMs and how this knowledge can be used to improve DRAM's reliability.**

Keywords—DRAM, Approximate DRAM, Reverse Engineering, Measurements

DRAM has to be refreshed regularly due to its charge-based bit storage property (capacitor). The retention time of a DRAM cell is defined as the amount of time that a cell can safely retain its data without being refreshed. It is a fact that 40% to 50% of power consumption in future 32- or 64-Gbit DRAMs has to be attributed to refresh commands. Moreover, 3-D-integrated DRAMs such as Wide I/O or hybrid memory cube worsen the scenario with respect to increased cell leakage due to the much higher temperature in 3-D stacks. Therefore, the refresh frequency must be increased to avoid data corruption. In recent years, the paradigm of approximate computing has been extended to the DRAM subsystem, called *Approximate DRAM*. The underlying motivation of this approach is to reduce the increasing power consumption caused by unavoidable DRAM refresh commands by lowering the refresh frequency or even disabling the refresh completely while accepting the risk of data errors. However, the amount of tolerable errors (resilience) strongly depends on the application. The degradation of the output quality of an application is directly related to the used DRAM device, the temperature, and the target application itself. Therefore, it is essential to truly investigate the DRAM retention errors before deploying it as approximate memory in specific applications. The aforementioned issues we address with DRAMMeasure, which is a low-cost DRAM power consumption and retention time measurement platform that outperforms state-of-the-art measurement systems. It consists of a FPGA board and two expansion *Printed Circuit Boards* (PCBs), one as an adapter for the small outline dual inline memory module (SO-DIMM) slot and another for temperature control and current sensing. With this measurement platform, we characterize the retention time behavior of different DDR3 and DDR4 DRAM devices from several vendors.

Furthermore, we show that DRAM's retention errors have an asymmetric behavior and we show how this asymmetry can be exploited in order to increase DRAM's reliability. Our proposed method is based on the observation that its more likely that a physical 1 in the DRAM can leak to a physical 0 ($1 \rightarrow 0$) than the other way around ($0 \rightarrow 1$). This error behavior is concealed by the vendor specific way of storing data in the DRAM, where some cells store the data as is, so a logical 1 is stored as a physical 1 (true-cells), and other cells store the data inverted, so a logical 1 is stored as physical 0 (anti- cells). With our measurement platform we are able to reconstruct the physical location of memory cells and the types (true or anti) in a DRAM without opening the device package and microscoping the device. Our method consists of a retention error analysis while a temperature gradient is applied to the DRAM device.

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