Architecture Evaluation Tool for 3D CAMs

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***Abstract*—Three-dimensional (3D) integration using through-silicon via (TSV) has been used for memory designs. Content addressable memory (CAM) is an important component in digital systems. In this paper, we propose an evaluation tool for 3D CAMs, which can aid the designer to explore the delay and power of various partitioning strategies. Delay, power, and energy models of 3D CAM with respect to different architectures are built as well.**

I. Introduction

Three-dimensional (3D) integration technology using through silicon via (TSV) has been used for optimizing the performance and power of DRAM [1]. Content addressable memory (CAM) is also a component having very high requirement on the performance and low power consumption. 3D CAM provides the possibility to meet the requirement. A typical CAM has the read, write, and compare (search) operations. The compare operation is the most critical operation on power and performance. While a compare operation is executed, the data on searchlines (SLs) are compared with the data stored in the CAM words in which each word exports the comparison result through its matchline (ML). Then, the comparison results of all words are evaluated by a hit signal generator and/or priority address encoder (PAE).

Cell-level and architecture-level 3D CAMs were reported in [2], [3]. The cell-level 3D CAM needs a huge amount of TSVs. In this paper, therefore, we only consider architecture-level 3D CAMs. Architecture-level 3D CAMs can be divided into searchline- and matchline-partitioned CAMs. Fig. 1 shows the two different 3D CAM architectures for an 8-word CAM. This paper presents an architecture evaluation tool for 3D CAMs. The architecture evaluation tool can provide the power and delay information with respect to different 3D CAM architectures.

II. Proposed Evaluation Tool for 3D CAMs

Different 3D architectures have different influences on the area, power, delay, and the number of required TSVs. Furthermore, either searchline-partitioned architecture or matchline-partitioned architecture can be designed with multiple layers. The number of layers has a heavy impact on the delay, power, and area of the 3D CAM. Therefore, an evaluation tool is developed for 3D CAMs, which can be used to aid the designer to select an appropriate architecture. Fig. 2 shows the conceptual diagram of the evaluation tool for 3D CAMs. Given the information of CAM cell structure and ML structure,

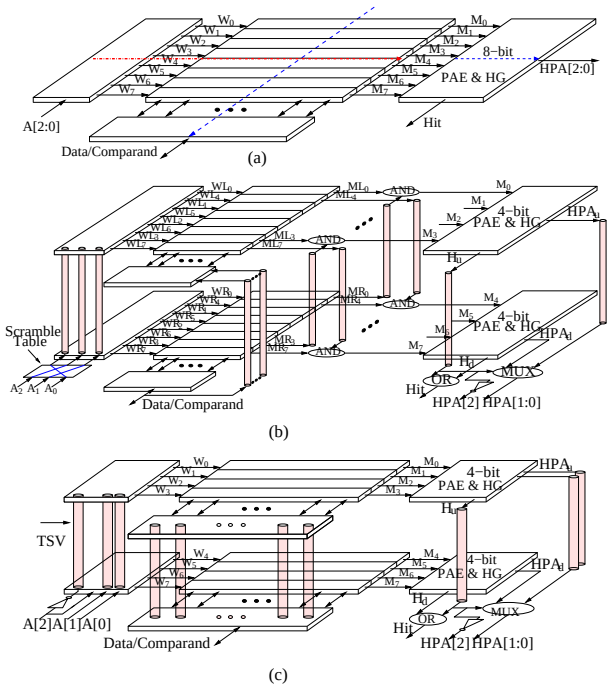

Fig. 1. (a) A 2D CAM with 8 words. (b) Searchline-partitioned 3D CAM with 2 layers and 8 words. (c) Matchline-partitioned 3D CAM with 2 layers and 8 words [3].

parameters of the 3D CAM, the number of partitions of MLs and SLs, the electrical data of used CMOS technology node, and TSV parameters, the evaluation tool can export the read/write delay, read/write power, search delay, search power, and TSV counts of the 3D CAM.

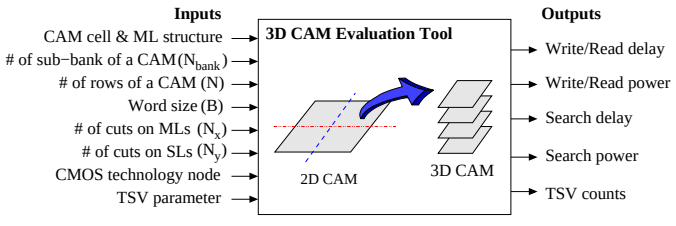

Fig. 2. Conceptual diagram of the proposed architecture evaluation tool for 3D CAMs.

Delay and power models of 3D CAMs are developed. Here, only the delay and power models of search operation are explained. Those for the other operations can be developed

in a similar way. The search delay model is shown as below.

$$T_{search} = T_{ML,pre} + T_{SL,drive} + T_{ML,eva} + T_{PAE}, \quad (1)$$

where $T_{ML,pre}$, $T_{SL,drive}$, $T_{ML,eva}$, and T_{PAE} denote the delay of per-charging ML, driving SL, evaluating ML, and PAE, respectively. Fig. 3 shows the modified RC models of SL and ML in a 3D CAM. According to the RC models, the delay of SL and ML for a 3D CAM can be calculated. If the CAM is divided into multiple active layers, the critical path of SL and ML in each layer can be shortened. The equivalent capacitance and resistance of ML and SL in each layer can be expressed as follows:

$$\begin{aligned} C_{ML} &= (B/N_x) \times (2 \cdot C_d + C_{wire,w}) \quad (2)\\ R_{ML} &= (B/N_x) \times R_{wire,w} \\ C_{SL} &= (N/N_y) \times (C_g + C_{wire,h}) \\ R_{SL} &= \frac{N}{N_y} \times R_{wire,h} \end{aligned}$$

The search power consumption of 3D CAM is mainly constituted by the MLs, SLs, the additional logic for 3D CAM, additional TSVs, and PAE, which can be expressed as follows:

$$P_{search} = P_{ML} + P_{SL} + P_{logic} + P_{TSV} + P_{PAE}. \quad (3)$$

The power consumption of each component can be calculated in terms of the switching activity, equivalent capacitance, voltage supply, and operating frequency.

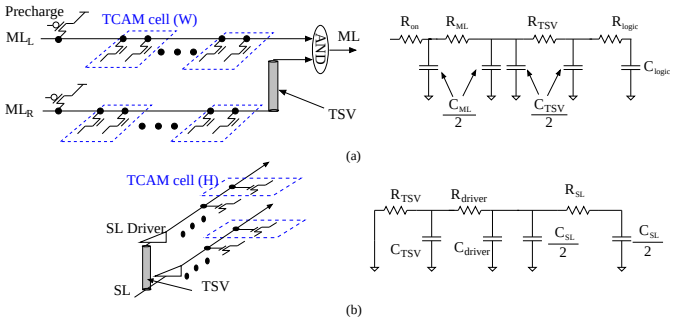

Fig. 3. RC models for (a) 3D ML search path and (b) 3D SL search path.

III. Simulation Results

Here we use the 65nm parameters according to the ITRS report [5] to evaluate different CAM architectures. Fig. 4 shows the the delay and power per search operation of a searchline-partitioned CAM (SPCAM) with respect to different numbers of SL partitions. As the number of SL partitions increases, we can see that the 256×128 CAM has significant reduction in search delay. The search power is increased as the number of SL partitions increases, because the total TSV counts and additional logic are also increases.

Fig. 5 shows the delay and power per search operation of matchline-partitioned CAM (MPCAM) with respect to different numbers of ML partitions. As the number of ML partitions increases, we can see that the 128×256 CAM has significant reduction in search delay. The search power is

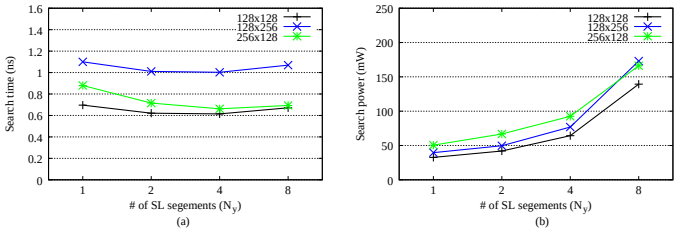

Fig. 4. Delay and power per search operation with respect to different SL partitions.

increased as the number of ML partitions increases, the reason is similar to the SPCAM.

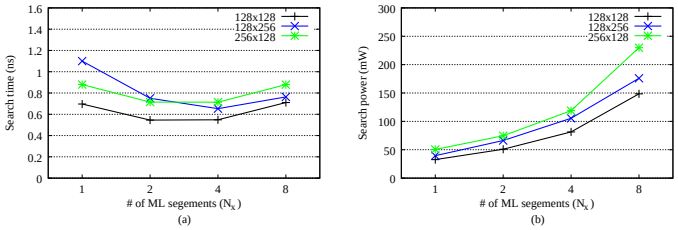

Fig. 5. Delay and power per search operation with respect to different ML partitions.

IV. Conclusions

In this paper, an architecture evaluation tool for 3D CAMs has been proposed. It can aid the designer to explore different possibilities for partitioning a CAM across multiple layers. Analysis results show that the search delay can be reduced using 3D stacking in comparison with the 2D technology. However, the search power is increased because of the additional capacitance of TSVs. Also, SPCAM is suitable for the application demanding large number of words, but MPCAM is suitable for the application demanding wide words.

Acknowledgment

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