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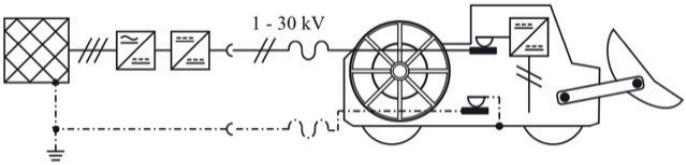

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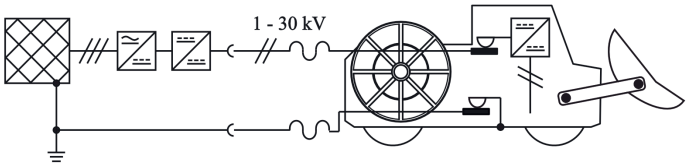

Modular High Voltage DC/DC Converters and Converter Control

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Stuttgart, in December 2022 Jochen Barthel

Abstract

Efforts in decarbonization lead to electrification, not only for road vehicles but also in the sector of mobile machines. Aside from batteries, those machines are electrified by tethering systems, nowadays featuring an AC low voltage system. Those systems are applied, e.g., to underground load haul dumpers with short tethering lines and low machine power. To expand tethering to further markets as agricultural machinery, this work proposes an HVDC tethering system allowing higher machine power and transmission length due to thinner, lighter tethering lines. The HVDC voltage is converted by distribution over a number of series connected DC/DC converters. Less blocking voltage on the semiconductors allows faster switching technology to reduce the converters' weight and volume. Since comparable concepts exist for offshore wind farms connectivity, its applicability for this is discussed. A full bridge inverter/rectifier LLC resonance DC/DC converter is presented for the modules. A switched LTI converter model is developed and a Common Quadratic Lyapunov Function (CQLF) is computed for prove of stability. The converter control features soft startup and voltage control over all modules. The concepts are validated by simulation and on a scaled prototype.

Kurzfassung

Die Bemühungen zur Dekarbonisierung führen zur Elektrifizierung, nicht nur bei Straßenfahrzeugen, sondern auch bei mobilen Arbeitsmaschinen. Neben Batterien werden diese durch Schleppleitungssysteme mit AC Niederspannung elektrifiziert. Solche Systeme werden z. B. bei Untertage-Radladern mit kurzen Leitungen und geringer Leistung eingesetzt. Um Schleppleitungen in weitere Märkte wie Landmaschinen auszuweiten, wird eine HVDC-Anbindung vorgeschlagen, die durch dünnere, leichtere Leitungen höhere Maschinenleistung und Übertragungslänge erlaubt. Die hohe Leitungsspannung wird durch in Reihe geschalteten DC/DC-Wandler aufgeteilt und gewandelt. Geringe Sperrspannung ermöglicht den Einsatz schnell schaltender Halbleiter, um Wandler-Gewicht und -Volumen zu reduzieren. Da vergleichbare Konzepte für Offshore-Windparks existieren, wird seine Anwendbarkeit für diese diskutiert. Für die Module wird ein Vollbrücken-LLC Resonanzwandler vorgestellt. Ein switched LTI Modell wird abgeleitet und die Stabilität durch eine Common Quadratic Lyapunov Function (CQLF) nachgewiesen. Die Spannungsregelung enthält eine Softstart Methode und Regelung über alle Module. Die Konzepte werden simulativ und prototypisch validiert.

Contents

List of Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
ASM	Asynchronous Machine
CO_2	Carbon-Dioxide
CQLF	Common Quadratic Lyapunov Function
DC	Direct Current
EMI	Electromagnetic Interference
EU	European Union
FHA	First Harmonic Approximation
HF	High Frequency
HIL	Hardware in the Loop
HV	High Voltage
HVAC	High-Voltage Alternating Current
HVDC	High-Voltage Direct Current
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
IT	Isolé Terre
LHD	Load Haul Dumper
LTI	Linear Time-Invariant
LV	Low Voltage
LVAC	Low-Voltage Alternating Current
MF	Medium Frequency
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MPC	Model Predictive Control
MPPT	Maximum Power Point Tracking
PCB	Printed Circuit Boards
PFC	Power Factor Correction
PID	Proportional-Integral-Derivative
PRC	Parallel Resonance Converter
PWM	Pulse Width Modulation
RMS	Root Mean Square
SISO	Single Input Single Output
SPICE	Simulation Program with Integrated Circuit Emphasis
SRC	Series Resonance Converter
zcs	Zero Current Switching
zvs	Zero Voltage Switching

List of Latin Symbols

Symbol	Description	Unit
$\boldsymbol{A}$	State matrix	
$\boldsymbol{A}_{\mathrm{NN}}$	Zero dynamics system matrix	
$\boldsymbol{A}_{1}$	State matrix for positive secondary current	
$\boldsymbol{A}_{-1}$	State matrix for negative secondary current	
$\tilde{\boldsymbol{A}}$	Preconditioned state matrix	
$f_{\mathrm{aw,min}}$	Anti-windup upper limit	Hz
$f_{\mathrm{aw,max}}$	Anti-windup lower limit	Hz
$\boldsymbol{A}_{0}$	State matrix for zero secondary current	
$\boldsymbol{b}$	Single-input state space input vector	
C	Capacitance	F
C_{GC}	Miller capacitance: Gate to collector capacitance of an IGBT	F
C_{GE}	Gate to emitter capacitance of an IGBT	F
c_{ies}	Total capacitance in a gate circuit capacitance	F
C_{in}	Input blocking capacitor	F
C_{o}	Output filtering capacitor	F
c_{os}	Parasitic output capacitance of a semiconductor element	F
C_{r}	Resonance capacitance	F
C_{rp}	Parallel resonance capacitance	F
C_{rs}	Series resonance capacitance	F
$\boldsymbol{c}^{\mathrm{T}}$	State space output matrix	
D	Diode	
Δf_{sw}	Inverter switching frequency range	Hz
d	State space transparency	
e	Control error	
e_{act}	Control error threshold for PID activation during startup	
f_{fb}	Feedback controller output frequency	Hz
f_{ff}	Feed forward controller output frequency	Hz
$f_{\mathrm{sw,min}}$	Minimal switching frequency	Hz
$\boldsymbol{f}_{\mathrm{sw,min}}$	Vector of minimal switching frequencies	Hz
$f_{\mathrm{sw,max}}$	Maximal switching frequency	Hz

Symbol	Description	Unit
f_n	Converter switching frequency, normalized versus the resonance frequency	1
$\boldsymbol{F}_\mathrm{n}$	Breakpoint matrix for the lookup table with normalized frequencies	1
$\boldsymbol{f}_\mathrm{n}$	Vector of equidistant, normalized frequencies	1
f_r	Resonance frequency	Hz
f_r1	Lower resonance frequency for resonance circuits with two resonance frequencies	Hz
f_sw	Inverter switching frequency	Hz
i_1	Transformer primary current	A
i_2	Transformer secondary current	A
i_C	Collector current	A
I_ds	Drain (so source) current	A
i_d	Diode current	A
i_Fe	Transformer core lose equivalent current	A
i_M	Transformer magnetizing current	A
I_max	Upper current limit	A
$I_\mathrm{Link,ref}$	Reference voltage for the electrical mobile machine's DC-link	A
I_o	Converter DC output current RMS value	A
i_o	Converter DC output current	A
i_r	Converter resonance current	A
I_RRM	Reverse peak current	A
i_sec	AC secondary current of the converter / transformer	A
I_tail	IGBT tail current	A
L	Inductance	H
L_1	Primary leakage inductance of a transformer	H
L_2	Secondary leakage inductance of a transformer	H
L_M	Transformer magnetizing inductance	H
L_n	Normalized inductance in an LLC resonance converter	H
L_r	Resonance inductance	H
L_rp	Parallel resonance inductance	H
L_rs	Serial resonance inductance	H
L_1tot	Total primary side inductance inductance	H
M_DC	Stationary, normalized converter DC gain	1
M_fha	Stationary converter gain of the FHA model	1
$M_\mathrm{fha,ext}$	Stationary converter gain of the extended FHA model	1
$\boldsymbol{M}_\mathrm{fha,ext}$	Matrix of stationary converter gain values of the extended FHA model	1
$\boldsymbol{m}_\mathrm{fha,ext}$	Vector of equidistant stationary converter gain values of the extended FHA model	1

Symbol	Description	Unit
$M_{\max}$	Maximal design value for the stationary converter gain	1
$M_{\min}$	Minimal design value for the stationary converter gain	1
M_{ref}	Converter gain, required to achieve reference output voltage	1
N	Total number of converter modules	
n	Transformer turns ratio	1
N_1	Number of transformer primary turns	1
N_2	Number of transformer secondary turns	1
$\boldsymbol{P}$	Arbitrary positive definite symmetric matrix	
p	Grade of the trajectory polynomial	
P_{Load}	Converter load power	W
$P_{\mathrm{Load,set}}$	Converter load set-point	W
P_{nom}	Nominal power	W
P_{v}	Power loss	W
$P_{\mathrm{v,D}}$	Power dissipation in a diode	W
$P_{\mathrm{v,full}}$	Conducting power dissipation in a full bridge	W
$P_{\mathrm{v,half}}$	Conducting power dissipation in a half bridge	W
$P_{\mathrm{v,Tfb}}$	Power dissipation in the converter secondary side with full bridge rectifier	W
$P_{\mathrm{v,Tct}}$	Power dissipation in the converter secondary side with center taped transformer	W
$\boldsymbol{Q}$	Arbitrary positive definite symmetric matrix	
Q_{e}	Primary side equivalent quality factor of a loaded LLC converter	1
Q_{e}	Quality factor of the FHA converter model	1
r	Relative grade of a dynamic system	
R_1	Resistance of the transformer primary side winding	Ω
R_2	Resistance of the transformer secondary side winding	Ω
R_{df}	Diode forward conducting resistance	Ω
R_{e}	AC side load equivalent resistance	Ω
$\boldsymbol{r}_{\mathrm{e}}$	Vector of AC side load equivalent resistance	Ω
R_{Fe}	Transformer core loss equivalent resistance	Ω
R_{L}	Load equivalent resistance	Ω
R'_{L}	Primary side transformed load equivalent resistance	Ω
R_{on}	Semiconductor switch on-state resistance	Ω
$R_{\mathrm{on,full}}$	Total R_{on} in the current path of a full bridge	Ω
$R_{\mathrm{on,half}}$	Total R_{on} in the current path of a half bridge	Ω
S	(Semiconductor) switch	
$\boldsymbol{S}_{\mathrm{B}}$	Observability Matrix of a System	
$\boldsymbol{S}_{\mathrm{S}}$	Controllability Matrix of a System	
t	Time	s

Symbol	Description	Unit
t_0	Start time	s
T_1	Transformer of the LLC resonance converter	1
t_d	Dead time between the on states of an inverter	s
t_e	End time instance of a transition	s
t_fade	Voltage fade out time	s
t_fi	Current fall time	s
t_fv	Voltage fall time	s
$t_\mathrm{on/off}$	Turn-on respectively turn-off time	s
t_ri	Current rise time	s
t_rv	Voltage rise time	s
T_s	Simulation / computation step size / Sampling time	s
$T_\mathrm{s,C}$	Sampling time of the control algorithm	s
$T_\mathrm{s,M}$	Sampling time of the converter's simulation model	s
$T_\mathrm{s,R}$	Sampling time of the simulation data recording	s
T_sw	Converter switching period at operating frequency f_sw	s
t_tail	Current tail time	s
u	SISO state space system input – Control value	
$V(\boldsymbol{x})$	Lyapunov function	
v_1	Input voltage of the converter's resonance network	V
v_2	Transformer secondary voltage	V
v_CE	Collector-Emitter voltage	V
V_CEon	Collector-Emitter on state saturation voltage	V
v_Cr	Resonance capacitor voltage	V
$\hat{v}_\mathrm{Cr}$	Resonance capacitor peak voltage	V
V_dc	DC voltage	V
V_df	Diode forward voltage	V
V_dr	Diode reverse blocking voltage	V
v_DS	Drain-Source voltage	V
$\boldsymbol{f}$	Vector field, general expression for a state function	
$V_{\mathrm{E},k}$	Electric base potential of the k^th converter module	V
V_f	Fundamental of the converter input square wave voltage	V
v_Fe	Voltage across the magnetizing core equivalent resistor	V
V_FRM	Turn-on voltage peak of the diode	V
v_GS	Gate-Source voltage	V
$V_\mathrm{in,min}$	Minimal DC input voltage for the DC/DC converter	V
V_in	Input voltage of an electrical network	V
$V_\mathrm{in,nom}$	Nominal DC input voltage for the DC/DC converter	V
$V_\mathrm{Line,n}$	Nominal tethering line voltage	V
$V_\mathrm{Line,ref}$	Reference voltage for the tethering line controller	V

Symbol	Description	Unit
v_{M}	Transformer magnetizing voltage	V
$V_{\max}$	Upper voltage limit	V
V_{Mod}	Terminal voltage of a converter module	V
$V_{\mathrm{Link,ref}}$	Reference voltage for the electrical mobile machine's DC-link	V
V_{o}	Output voltage of an electrical network	V
V_{oe}	Primary side transformed converter load RMS voltage	V
$V_{\mathrm{o,inf}}$	Finite value of a stabile output voltage	V
$V_{\mathrm{o,min}}$	Minimally achievable output voltage of the DC/DC converter	V
V_{on}	Device on state voltage drop	V
$V_{\mathrm{o,nom}}$	Nominal output voltage of the DC/DC converter	V
$V_{\mathrm{o,ref}}$	Output voltage reference value	V
$V_{\mathrm{r,in}}$	Input voltage of a resonance circuit	V
$V_{\mathrm{r,o}}$	Output voltage of a resonance circuit	V
$\bar{w}_{\mathrm{e}}$	End value of a trajectory for a system transition	
$\bar{w}_0$	Start value of a trajectory for a system transition	
$W_{\mathrm{on/off}}$	Turn-on respectively turn-off energy dissipation	J
w	Reference trajectory for an output transition	
$\boldsymbol{x}_{\mathrm{e}}$	Equilibrium Point of a system	
$\boldsymbol{x}_{\mathrm{N}}$	Zero dynamics states	
$\boldsymbol{x}$	System states vector	
y	Output variable in a state SISO state space system	

List of Greek Symbols

Symbol	Description	Unit
δ	Number of any non-infinite size	
ΔM_{G}	Operative range of gain of a DC/DC converter	1
ΔP_{Load}	Defined converter load range	W
ΔV_{p}	Voltage overshot	V
ϵ	Arbitrarily low number of any non-zero value	
σ	State matrix switching parameter	

1. Introduction

Electrical power transmission and conversion experiences a continuously increasing relevance in academia and industry due to constantly growing demand of electrical energy in nearly every aspect of life. Additionally, efforts to reduce Carbon-Dioxide (CO_2) emissions and other environmental protective aspects, result in constantly tightening emission regulations for a vast number of applications throughout the world. In the electrical energy generation sector, this leads to a changing situation due to decentralization by a growing share of renewable energy sources. Additionally, electrification of further applications, e.g., from the transportation sector and mobile machinery, adds to the growing demand for electric energy and the increased research interest. Regarding mobile machinery, as of the year 2010, in the European Union (EU) non-road mobile machinery contributed 2 % of the Unions total CO_2 emission [VVHFF10].

Decentralization of the electrical energy generation and increased energy demand lead to more dynamics in the electric energy transmission paths and transmitted power in the energy transmission grid. The dynamics are induced due to the higher volatility of the renewables: if one renewable energy source produces high excess supply in one region, this will be transmitted to a region, where the demand exceeds the current generation capacity. While the transmission amount and direction are subject to a highly dynamic process in such a system, the energy transmission paths in a classical supply grid are not static but still far less dynamical. Second, the energy supply of systems as electrified vehicles of all kind or mobile machines display additional loads of significant measure, which further stresses the grid. In response, transmission technology and energy conversion techniques are under research with respect to meet these changing requirements.

The following sections will briefly set the topics of electrical energy transmission and electrical energy conversion in the context of its current utilization. Transmission and conversion techniques and their applications are sketched out and chances, offered by Modular High Voltage (HV) DC/DC Converters are motivated. This introduction closes with an outline of this theses.

1.1. Electrical Energy Transmission

In a classical grid, electrical energy is transmitted from the electrical power plant to the consumer via a High-Voltage Alternating Current (HVAC) grid. At the power plant site, the voltage is transformed to HV with a transformer, fed into the grid, transmitted to the consumers region, where it is transformed back to Low Voltage (LV) and fed to the LV distribution grid. This method is known as HVAC transmission, voltages up to $400\,\mathrm{kV}$ are commonly used in Europe. Transformation to and from HVAC with transformers is a long known, relatively cheap technique. Losses on the transmission line are considerably low, but due to the capacitive nature of the transmission lines, reactive losses occur, that lead to an over proportional increase of transmission loss with increasing distance. This fact limits the economically reasonable maximal transmission voltage and distance. In literature, HVAC transmission is considered economically reasonable for distances up to a few hundred km [KSW13, Ch. 7.2], [OO11, Ch 19.5].

To connect, for example power plants in remote areas or offshore wind farms to the electric grid, HVAC transmission quickly reaches its practicable limits, due to the above discussed loss to distance relation. In such cases, High-Voltage Direct Current (HVDC) transmission is applied, where the source power is transformed, rectified and fed to the transmission line in Direct Current (DC) form. The DC transmission line represents a point-to-point connection. On its end the current is inverted back to Alternating Current (AC), transformed and fed to the HVAC grid. Within HVDC transmission, no reactive losses exist and hence, voltages up to some MV are possible. Since the majority of the cost and the losses occur in the head stations and HVAC is reasonably cheap on short distances, HVDC transmission is mainly applied for distances above $1000\,\mathrm{km}$, where it is more economical than HVAC and for sea cables – where the parasitic capacitance per meter is large – above $40\,\mathrm{km}$ [Sch12, Ch. 10]. With the rising growth of the renewable energy generation sector and the corresponding increasing distance between power source and sink, HVDC transmission becomes more and more interesting for academia and industry.

Besides the energy sector, a second application, where high electric power has to be transmitted is that of tethered mobile machines, namely in the open pit and underground mining industry [YFM09, JHB14]. In the state-of-the-art setup, these machines, like large excavators and LHDs, have a reel installed on the body, whereon a tethering line is stored. The schematical setup of the power supply of such a tethered mobile machine is given in Figure 1.1. On the operating site, a $50\,\mathrm{Hz}$ or $60\,\mathrm{Hz}$ three-phase transformer isolates the site's energy supply net versus earth potential, forming an Isolé Terre (IT)-net. The machine is connected to the site's net via a reelable,

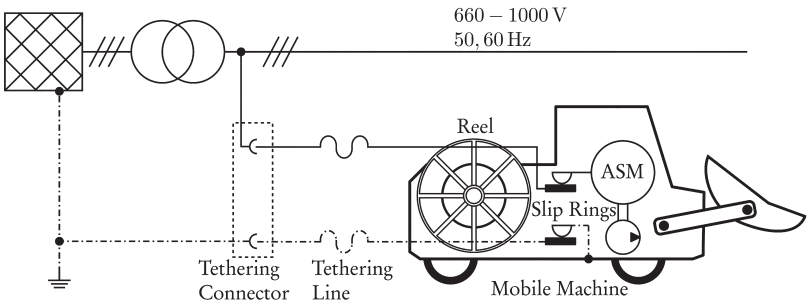


Figure 1.1.: Schematics of the power supply of a tethered machine on the example of an electrical underground mining Load Haul Dumper (LHD).

flexible tethering line, which is stored on a reel on the LHD. From the reel, the energy is transmitted to the machines electric drives via a set of slip rings. The drives – here depicted in the form of an Asynchronous Machine (ASM) – usually power hydraulic pumps for the bucked operation, moving power, etc.. The power is transmitted in AC machine voltage level, which requires thick and heavy tethering lines, even for low power. The machine's action radius arises from the available tethering line on the reel. For current machines with Low-Voltage Alternating Current (LVAC) supply, this is limited to a few hundred meters due to the thick LV lines [JHB14]. To increase the power, that can be installed on such a machine and/or the possible operating radius without reconnecting the tethering line to another connection point, the transmission systems power density must be increased. Therefore, the most promising option is increasing the transmission voltage. Increasing the power density could possibly be an enabler to apply tethering systems to more mobile machines – also in further industries.

1.2. Electrical Energy Conversion

Electrical energy converters are widely used in many different applications, like electric power generation and transmission, electric motor applications and the voltage supply of many end devices. Converters for AC to AC (transformer / frequency converter), DC to DC (DC/DC converter), AC to DC (rectifier) and vice versa (inverter) exist. The converter power ratings reach from few mW up to the multi-MW range. Especially in high power applications, conversions between different voltage levels are often implemented with a transformer to obtain a more stable design and in some application

cases to isolate the different grids from each other. In some applications it is necessary to operate transformers in higher frequency to safe installation space and weight. For simple rectification, diode rectifiers can be utilized, however for higher conversion power, rectifiers with active Power Factor Correction (PFC) technologies are used to reduce Electromagnetic Interference (EMI) emissions (e.g., distortion reactive power) to the AC grid. In (two phase) inverters, electronic switches like Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) or Insulated Gate Bipolar Transistors (IGBT) are arranged and driven in a way, such that the positive DC voltage is alternately conducted to the two conductors of the (AC) output – it is the inverse operation of a rectification.

In recent years, some trends with positive influence on research efforts in power converter technology can be observed. One is the increasing use of renewable energy and the therewith ongoing growth of the market for HVDC transmission, where high-voltage and high-power power converters are required [HBM+13, MP15]. Second the growing interest in electrification in the automotive industry and for mobile machinery pushes the inverter and DC/DC converter technology [PTB10, SEMR+15, SJB15]. Major research goals are increased efficiency, reliability and power density [DBK12, LL10, MLC+08]. To keep stress of the grid by harmonic distortion and reactive power low, the improvement of the waveform quality for grid connected converters becomes more relevant with increasing number and power rating and hence, is subject to research and must comply with legal regulations and valid standards e.g., *EN 50160:2010 Voltage characteristics of electricity supplied by public distribution networks* [CEN10], [Ank00, Ch. 10].

To meet these given development objectives, one major focus lies in the improvement of the physical characteristics of the converter components. Ohmic losses are reduced and fast switching capabilities are increased. For high-voltage applications, efforts to increase the maximal blocking voltage of semiconductor switches are undertaken. The current limit for commercially available IGBTs lies at 6.6 kV, in research, blocking voltages as high as 13 kV are reported [CRC+09]. For a few years, on the circuit side, resonance switching techniques are state-of-the-art in commercially available power converters. In such converters, resonance circuits are excited in the vicinity of their characteristic frequency, generating a waveform that allows the semiconductor switches to be turned on and off close to the zero-crossing instance of the oscillation. This technique leads to quasi-lossless operation with significantly reduced stress to the semiconductor components and EMI emissions. This loss and stress reduction enables more efficient, faster converter operation and can increase its robustness. Higher frequencies reduce the size and weight of passive components, so that higher volumetric and gravitational power densities can be achieved. With smaller passive

components, usually the cost can also be reduced, contrary, fast switching capable semiconductors might counteract the economical goal.

For power conversion at the endpoints of HVDC transmission lines, converters with a structure, that is known as multilevel converter is presented in literature and is commercially available. The key in these converters is the division of the terminal voltage to series connected power semiconductor switches. By the voltage division, voltages, that are higher than the blocking voltage of a single semiconductor switch can be handled. This splitting of the voltage to the semiconductors can be achieved for example with diodes (e.g., diode clamped converter) ore capacitors (flying capacitor, modular multilevel converter). For example, a brief review on existing multilevel inverter topologies is given e.g., in [Mün11].
A further field of application, where high voltage is divided over a number of semiconductor switches are electrical railway traction systems, it is also described in [SR07, MLC+08]. From the catenary wire, a number of full bridge rectifiers are connected in series at their AC terminals, each rectifier output feeds into a separate low voltage DC link. From there, DC/DC converters with magnetic coupling generate the voltage for the drive systems. Here the magnetic coupling ensures that the voltage drop across the input semiconductors is leveled out.[MLC+08] For high power DC/DC applications, a patent [Rei02] describes a setup, where the DC capacitors of DC/DC converters form a capacitive voltage divider. The voltage dividers outer terminal is connected to the high voltage output terminal.
For the connection of high-power offshore wind farms to the HVDC line, new distributed converter concepts based on DC/DC converters are discussed in academia for a few years already, e.g., in [HJSK11, MP15]. In the given references, it is proposed to series connect the DC output of the single wind turbines and thereby form the high DC voltage for transmission to shore. This way, the complexity of the single wind turbines increases, but the need for a central conversion station is obsolete.
Even though the described systems greatly differ from each other, they all have in common, that a voltage, that is too high to be switched by one semiconductor switch, is distributed over a number of semiconductors and that high frequency is applied for voltage conversion.

1.3. Motivation and Objectives of this Publication

With this publication, the concepts from literature regarding high voltage power converters with modular structure is picked up and brought into a form, where it is suitable to be installed on a tethered mobile machine. The goal is to show, that with a DC/DC converter with a compact design, a mobile machine can be tethered by

HVDC. This way, the total tethering systems power density is increased and either more tethering line or more machine power can be installed on the machine. Both are key factors to spread tethered machinery technology to further industry sectors. With the chosen approach, the high tethering line voltage is distributed between a number of converter modules. The then small maximal voltage on one module (semiconductor switch) allows the utilization of semiconductors with fast switching capabilities. In combination with state-of-the-art resonance switching technologies, high power densities can be achieved and high power ratings are implementable on the very limited space of a mobile machine.

The publication is outlined as follows. In the following Section 2, the state-of-the-art of resonant switched DC/DC converters are outlined, an in-detail view for LLC converters is given, control methods for DC/DC converters are briefly discussed and the theory on linear switched systems is summed up. Section 3 justifies the converter architecture and closes with example applications, once, for an offshore wind farm power conversion and second the implementation of a HVDC tethering system on a mobile machine. Mathematical system analysis and controller design on module and system level are located in Section 4. In Section 5, results from simulation and measurements from a scaled prototype are given. The publication is closed with a conclusion of the work and an outlook to new perspectives in Section 6.

2. State-of-the-Art of Resonant Switched DC / DC Power Converters

The input inverter of conventional switched mode DC/DC converters is driven by Pulse Width Modulation (PWM) in hard switching mode. With the hard switching technique, the semiconductor switches are forcefully turned on, while the full rated voltage is applied to them and forcefully turned off, while the full rated current runs through them. Output voltage and current are rated by variation of the inverter duty cycle and therewith by the voltage-time-integral. This operating scheme allows compact converter designs with good efficiency, mayor losses occur during switching of inductive loads in the switched semiconductors. Contrary, hard switching operation of semiconductor switches in circuits with inductive components induces stress by voltage and current peaks during turn-off and -on, respectively. These peaks and sharp edges during switching results in high EMI [MUR03, Ch. 9] [Lut12, Ch. 6].

In the following chapter, methods to further improve the converter operating characteristics are discuses and a survey over the state-of-the-art of these techniques, namely zero voltage / zero current switching, is given. In the second part of this chapter, resonant DC/DC converter topologies with one, two and three resonant elements are given and state-of-the-art modeling and design methods are discussed. For the converter operation, an overview over control strategies from literature for DC/DC converters in general and resonant converters in particular are given. If not otherwise specified, in the following content, it will be taken as given, that IGBTs are utilized for power semiconductor switches in the converters.

2.1. Zero Voltage / Zero Current Switching

The goal in soft switching is to turn on the semiconductor switch under zero voltage condition, where the voltage drop across the switch is neglectable, and turn it off under

zero current condition, when no or little current flows through the semiconductor. The concept of Zero Current Switching (zcs) in power converter circuits reaches back to the early 1970s [Sch70], the one of Zero Voltage Switching (zvs) back to the late years of the same decade [KSY79]. Towards hard switching operation, these techniques aim improvements in a number of physical effects, as power dissipation and EMI.

2.1.1. Switching behavior and losses in IGBTs

The thermal energy, lost in the current carrying path during a turn-on or -off transition of an IGBT is given by

$$W_{\mathrm{on/off}} = \int_{t_0}^{t_{\mathrm{on/off}}} \left(v_{\mathrm{CE}}(t) i_{\mathrm{C}}(t)\right) \mathrm{d}t, \tag{2.1}$$

where $W_{\mathrm{on/off}}$ is the lost energy during turn-on or -off, respectively. v_{CE} is the collector to emitter voltage and i_{C} is the collector current of the IGBT. The respective transition for turn-on or -off starts at time t_0 and ends at $t_{\mathrm{on/off}}$. The typical voltage and current waveforms during hard switching turn-on and -off transitions are visualized in the middle diagram of Figure 2.1, the top diagram shows the corresponding IGBT Gate-to-Source voltage v_{GS} and in the lower diagram, the power dissipated in the semiconductor's channel is given. The individual sections and their physical correlations are well described in literature like [MUR03, Ch. 25] and [Lut12, Ch. 3]. From the waveform in the figure, it can be observed, that during turn-on, the current rises, before the voltage starts falling to its on-value V_{CEon} during the conducting phase and during turn-off, the voltage rises to the blocking voltage before the current begins to fall. This results in the power dissipation peaks, displayed in the figure during turn-on and -off.

For an IGBT in a circuit with inductive load, according to [Lut12] and the piecewise integration of the turn-on time interval from Figure 2.1 according to equation (2.1), the dissipated turn-on energy per pulse resolves to

$$W_{\mathrm{on}} = \frac{1}{2} V_{\mathrm{dc}} (i_{\mathrm{C}} + I_{\mathrm{RRM}}) t_{\mathrm{ri}} + \frac{1}{2} V_{\mathrm{dc}} (i_{\mathrm{C}} + \frac{2}{3} I_{\mathrm{RRM}}) t_{\mathrm{fv}} + \frac{1}{2} V_{\mathrm{CEon}} t_{\mathrm{fade}}, \tag{2.2}$$

where V_{dc} is the DC voltage applied to the circuit, I_{RRM} is the reverse peak current of the freewheeling diode and V_{CEon} is the on voltage drop of the channel. The time intervals are t_{ri} for the current rise time, t_{fv} for the voltage fall time and t_{fade} for the voltage fading to V_{CEon}. [Lut12] The first two summands correspond to the fact that the device current rises before the voltage starts falling, these two contribute

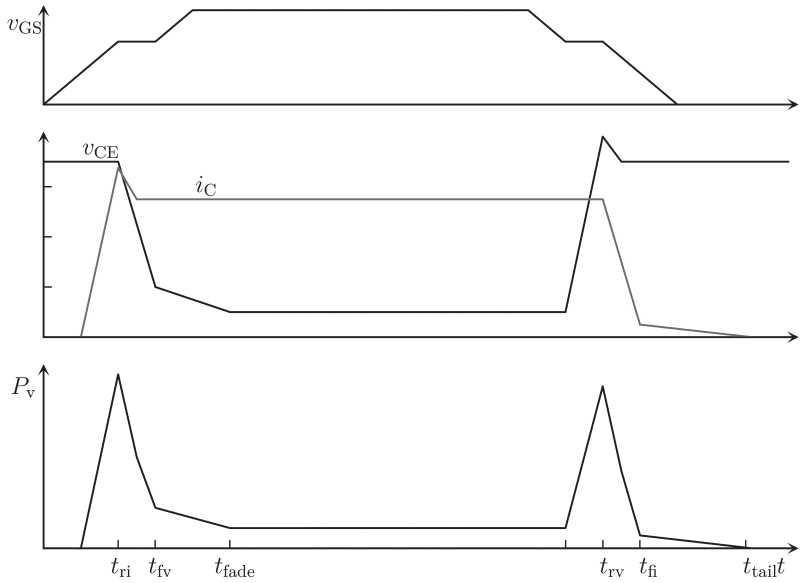


Figure 2.1.: Typical simplified voltage and current waveforms and corresponding power dissipation of an IGBT

the majority of the total turn-on losses in hard switching condition. The height of the peak current I_{RRM} is proportional to the current rise $^{di}/_{dt}$ and the strength of i_C in conducting mode, which leads to additional stress to the IGBT and high EMI radiation. Respective to the turn-on losses, the integral for the turn-off loss yields

$$W_{off} = \frac{1}{2} V_{dc} i_C t_{rv} + \frac{1}{2}(V_{dc} + \Delta V_p) i_C t_{fi} + \frac{1}{2} I_{tail} V_{dc} t_{tail}, \tag{2.3}$$

with the voltage peak ΔV_p and the tail current I_{tail}. The time intervals correspond to the voltage rise time t_{rv}, the current fall time t_{fi} and the tail current time t_{tail}. [Lut12] Corresponding to the turn-on losses, the first two summands contribute the majority to the hard switching energy loss, however the loss, caused by the tail current is larger than the one caused by the voltage fading. The voltage overshoot is proportional to the current i_C and the voltage rise factor $^{dv}/_{dt}$ roots in the inductances of the current path.

On the gate side of a MOSFET or an IGBT, the loss roots from the repetitive charging and discharging of the input capacitance $c_{ies} = C_{GE} + C_{GC}$. The gate

Table 2.1.: Operating frequency limits of semiconductor switches for hard- and soft switching methods [WNTR15, p. 275]

Semiconductor Switch Type	*Maximal Operating Frequency*	
	Hard Switching	*Soft Switching*
MOSFET	100 kHz	250 kHz
1200 V-IGBT	20 kHz	150 kHz
1700 V-IGBT	10 kHz	150 kHz

charge current repetitively flows through the gate resistor and through the upper and lower driver transistor, while charging and discharging respectively and by this emits charging losses. [WNTR15]

To reduce the switching losses, the area under the power curve in Figure 2.1 must be reduced. In hard switching operation, this would mean, that the rise- and fall times of voltage and current in the switching instance must be reduced to reduce switching losses. The time intervals t_{ri} and t_{fv} at turn-on as well as t_{rv} and t_{fi} at turn-off are approximately proportional to the IGBT gate resistance and can be reduced, to a certain degree, by the use of a lower gate resistance. [Lut12, WNTR15] The time intervals t_{fade} and t_{tail} cannot be influenced. A reduction of these discussed time intervals, would reduce the results of equations (2.2, 2.3) and hence the switching losses. While the goal of reducing losses is reached in the switches, the losses in the reverse diodes are increased [WNTR15]. The voltage overshot

$$\Delta V_{\mathrm{p}} = L_{\mathrm{par}} \frac{\mathrm{d}i_{\mathrm{C}}}{\mathrm{d}t} + V_{\mathrm{FRM}}, \tag{2.4}$$

is proportional to the steepness of the current falling slop $^{\mathrm{d}i_{\mathrm{C}}}/_{\mathrm{d}t}$ and the turn-on voltage peak of the diode V_{FRM} and hence, will be increased by reducing the switching time. The increase of the overshot and the steeper current and voltage slopes generate stronger undesirable EMI and component stress [Ank00, p. 321]. Hence, increasing the switching transient time does not lead to improved overall switching behavior.

The discussed effects of hard switching on efficiency, EMI and component stress are the major motivations to develop methods, where the collector-emitter voltage drops preferably to zero, before the collector current starts rising during the turn-on transition and vice versa, the current drops to zero, before the voltage rise starts at turn-off. Further, with reduced switching losses per transition, the operating frequency of power electronic circuits can be increased without increasing the overall thermal

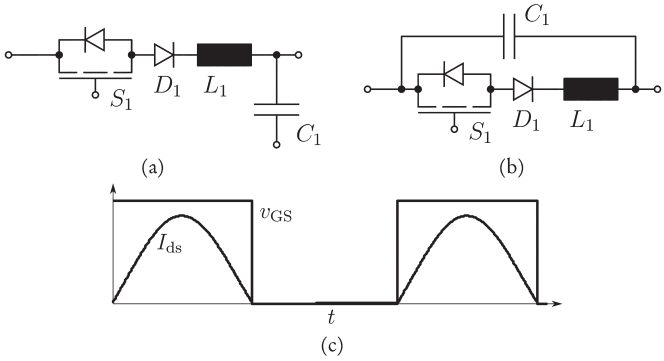


Figure 2.2.: L-type (a) and M-type (b) zero current switch in accordance to [LL84]. Subfigure (c) displays the switch control voltage and switch current of a buck converter with zero current M-type switch.

stress on the switched semiconductors. As a consequence, increased frequencies lead to smaller passive components and hence more compact and often more cost-efficient converter designs. Table 2.1 recites an overview of switching boundaries for hard- and soft switching frequencies for a selection of power semiconductor switches, especially IGBTs profit from soft switching operation by increased operation frequencies. [MUR03, p. 251] [WNTR15, p. 273] Soft switching is gained by the zcs and zvs, the transient behavior of both is discussed in the following sections.

2.1.2. Zero Current Switching

An early description of zcs was published in 1970 by Schwarz [Sch70]. In his publication a Series Resonance Converter (SRC) with a thyristor half bridge inverter is presented, where an LC series resonant circuit in the primary side, forms an appropriate current wave form to turn on the thyristors under zero current condition. In the following decade, Liu et al. presented two types of zero current switches and experimentally demonstrated its functionality with MOSFETs [LL84]. The schematics of the L- and M-type switching networks, presented by Liu et al., are given by Subfigure 2.2a and 2.2b, respectively. The circuits consist of a semiconductor switch S_1, an inductance L_1 and a capacitor C_1. If the switch has a free-wheeling diode – like in the Figure – a serial diode D_1, reversely polarized to the free-wheeling diode must be installed to block the reverse current path through the freewheeling diode. The current I_{ds} of a zero current MOSFET switch with its gate voltage v_{GS} is plotted in

Subfigure 2.2c. When the switch is turned on, the current describes a quasi-sinusoidal half-wave form, there is no instantaneous current rise, the switch is turned on at zero current. While conducting, the current rises to its maximum and drops back to zero, where the switch is turned off under zero current condition. For further details on L- and M-type zero current switches refer to [LL84]. With the described circuits, zcs is possible and the $^{di}/_{dt}$ is reduced in the switching network, but the voltage waveform still contains sharp edges, hence, EMI issues are reduced, but still remain.

The internal dynamics of an IGBT, turned off under zero current condition was investigated by Trivedi et al. in [TS99]: When an IGBT is turned off at zero current, a large amount of excess charge remains inside the semiconductor, at hard turn-off, this charge forms the IGBT-specific tail current. During the following time, this remaining charge decays partly by recombination and mainly by equal electron and hole currents inside the semiconductor. When the external voltage rises high enough, the remaining charge is swept out. Due to the minor remaining charge at the instance of the voltage rise time, this part of the turn-off losses is lower than the hard switching turn-off loss part of the tail current in equal system configuration but non-zero.

2.1.3. Zero Voltage Switching

To achieve zero voltage switching in practice, the current is commutated to the antiparallel diode of the semiconductor switch. Then, the voltage drop across the switch is equal to the voltage drop of the conducting diode – which is near zero – and the switch is turned on. After the current is reversed, it commutates from the diode to the already fully conducting channel. Two switching networks for zvs are presented in [LL90], that are similar to the zcs switch from section 2.1.2. The half-wave mode switches, given in the reference, are shown in Subfigure 2.3a and 2.3b respectively. Refer to the reference for the full-wave setup of these switching circuits. In both switching networks, one terminal of the capacitor is connected between the semiconductor and the inductance. The capacitor, that is connected directly to the switch terminals, shapes an appropriate voltage waveform to turn on the semiconductor at zero voltage, as displayed for the example of a MOSFET switch in part (c) of the figure. In the instance of turn-off of the MOSFET, its drain-source voltage v_{DS} is zero. After the zero-voltage turn-off, v_{DS} starts to describe a quasi-sinusoidal wave form, rises to its maximum and falls back to zero before the end of the off-time of the device. At the end of the off-time, v_{DS} is still zero and the MOSFET can be turned on under zero voltage condition. Liu et al. also state, that the junction capacitances are already discharged at switching time, which further reduces the switching losses in the channel. [LL90]

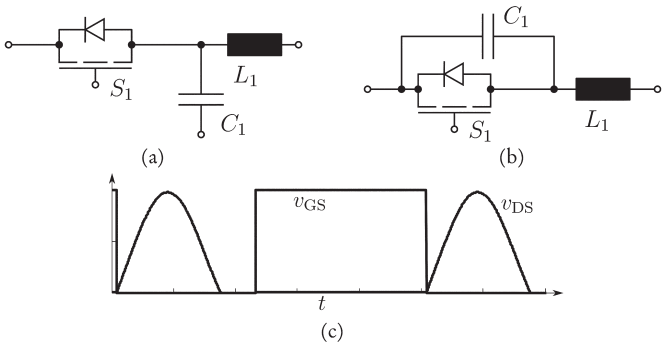


Figure 2.3.: Half-wave mode L-type (a) and M-type (b) switches for zero voltage switching according to [LL90] Subfigure (c): Switch control voltage and switch voltage drop of a zero voltage M-type switch in a boost converter.

At zero voltage turn-off of IGBTs, the remaining charge in the device causes a current bump with following tailing current. At the same time, the emitter-collector voltage starts to rise and power is dissipated. Compared to zcs, the distinct existence of current tails leads to higher losses in zvs-circuits with IGBTs. Contrary, circuit design is simpler and component values are smaller for zvs designs. [TS99] Zvs turn-on and quasi-zcs turn-off for IGBT was experimentally evaluated by Pavlovsky et al. [PdHF06]. Concordant to the effects, described in [TS99], the lowest turn-off loss was measured in devices with very small tail currents.

2.2. Resonant Switched Converters

The zero current and zero voltage switches described in the forgoing sections can be used for zcs / zvs in buck- and boost-type converters with one single switch (see [LL84, LL90]). For converter types with half- or full bridge inverter and rectifiers, it appears more suitable to approach this subject more comprehensively. However, the insights from the previous sections still hold their significance: To enable zvs and / or zcs, an appropriate waveform must be formed, ideally, for zvs the voltage, and for zcs the current, should be close to sinusoidal. To achieve these wave forms, a resonance circuit – also known as resonance tank – is formed with one, two or three energy storage elements e.g., capacitors and inductors. Due to their specific switching circuits, these converter types are also known as *resonant switched converters* or *resonance converter*.

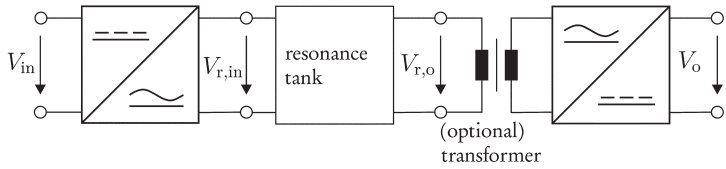
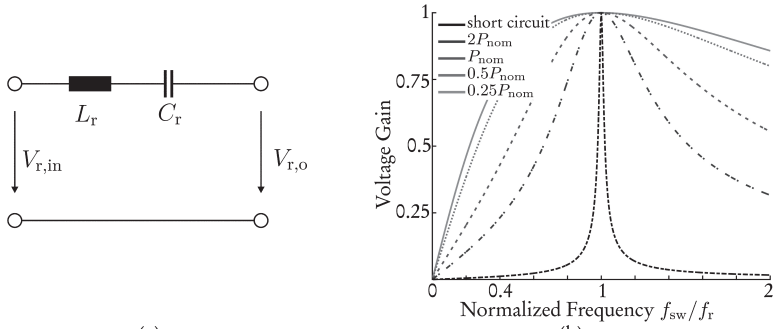


Figure 2.4.: Structure of a resonance DC/DC converter with input inverter, resonance tank, optional transformer and output rectifier

Resonance converter topologies can be classified by different characteristics. The most common classifications are the arrangement of their energy storage elements, e.g., series-, parallel connected [Yan03, p. 95 – 106], and by the number of their storage elements, respectively their number of resonance peaks [Bat94].

The common structure of a resonance converter is given in Figure 2.4. The DC input voltage V_{in} is inverted by a half- or full bridge inverter. The resonance tank, consisting of two, three or four energy storage elements, is excited by the resonance tank input voltage $V_{r,in}$, which is the output of the inverter. The converter may have an optional transformer to adept the converters output voltage to a desired voltage range. If a transformer exists, the resonance tank output voltage is applied to it, else, it is fed to the rectifier. The rectified and filtered converter output is the DC voltage V_o. For the following discussions, it appears handy to focus on the analog filter characteristic of the resonance circuit to describe its effect on the converter voltage gain at varying inverter switching frequency. The damping behavior of this filter is influenced by the converter load, incoherently off the resonance tank topology, higher loads affect stronger damping behavior. Hence, the output voltage of a certain resonance tank depends on the switching frequency and the converter load. Typically, the output voltage regulation is accomplished by the variation of the switching frequency. The voltage gain characteristics of resonant converters are typically visualized by their steady state voltage gain characteristics, where the ratio between the resonance tank input and the output voltage is drawn over the operation frequency at various loads.

In the next subsections, resonance converter topologies will be classified by the number of their resonance peaks, and topologies with one, two and three resonance peaks will be introduced and briefly discussed. In topologies with more than one resonance frequency, f_r always denotes the resonance frequency at full load. Following, a more detailed insight into the LLC converter topology will be given. A comprehensive survey over resonance tank layouts with two, three and four storage elements is given in [Bat94].



(a) (b)

Figure 2.5.: Resonance tank (a) and voltage gain diagram (b) of a LC series converter

2.2.1. Single Resonance Circuits

The energy storage elements in a single resonance circuit can be arranged, for instance, in series with the resonance tank output. This layout is known as Series-loaded or SRC [MUR03, Ch. 9]. A series resonance tank, formed of a capacitor C_r and an inductor L_r is depicted in Figure 2.5a. The converter voltage gain is defined as the ratio between the resonance tank input- and output voltage, $V_{r,in}$ and $V_{r,o}$, respectively and is commonly plotted over the normalized frequency f_{sw}/f_r. The associated voltage gain diagram for steady state operation at different loads over the switching frequencies is given in part (b) of the Figure. For simplicity, the resistive power loss in the resonance circuit is commonly neglected. [MUR03, Yan03]

The resonance tank acts as an analog filter with variable resistive load, which can be mathematically described in the Laplace domain by the voltage gain function

$$G(s) = \frac{s}{\frac{L_r}{R_L}s^2 + s + \frac{1}{R_L C_r}}, \tag{2.5}$$

where R_L represents the converter load. It can be seen in the equation, that the resonance circuit is a second order bandpass filter with the eigenfrequency $f_r = 1/2\pi\sqrt{L_r C_r}$. By variation of the inverter switching frequency, the impedance of the filter varies and reaches its minimum at its eigenfrequency. The voltage gain diagram in Figure 2.5b shows the dependency between increasing load and decreasing damping behavior, further, it can be seen, that the gain never exceeds 1. The gain curves for all loads show rising slopes for switching frequencies below and falling slope above resonance. At resonance frequency, the gain is 1 for all load cases, which is the highest gain for

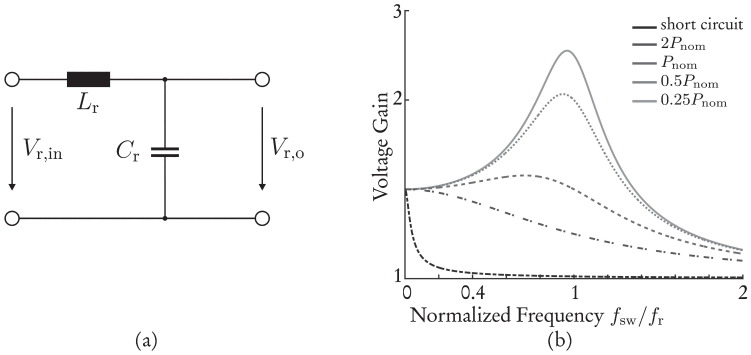


Figure 2.6.: Resonance tank (a) and voltage gain diagram (b) of a LC parallel converter.

SRCs. The described relations between load, frequency and damping can also be approached by physical interpretation. At resonance, the impedance of the filter is zero and all voltage drops at the load. Above and below resonance, the load voltage is proportionally divided to the impedance of the filter elements and the converter load. At switching frequencies below resonance, the phase of the filter is positive allows zcs. While the switching frequency approaches the gain peak, the phase decreases to zero, above the peak, at falling slope, the phase is negative and zcs is achieved.

If the output is utilized parallel to the capacitor of a second order resonance tank with an inductor in series with a capacitor, it is commonly known as Parallel Resonance Converter (PRC) [Ank00, Yan03]. The corresponding resonance tank layout and voltage gain curves are given in Figure 2.6. The voltage gain function in the Laplace domain is

$$G(\mathrm{s}) = \frac{1}{L_\mathrm{r} C_\mathrm{r} \mathrm{s}^2 + R_\mathrm{L} L_\mathrm{r} \mathrm{s} + 1}. \tag{2.6}$$

From the schematic in part (a) of the Figure and the gain function, it is obvious, that the resonance tank is a second order low pass. The gain curves for light load, which is equal to low damping, show rising slops and gain amplification towards the eigenfrequency. For increasing load, respectively damping, C_r is more and more bypassed by the load. Hence, the peaks shift towards smaller frequencies, the achievable amplification decreases and at short circuit condition only falling slopes appear. Like in the SRC, rising slopes correspond to zvs and falling to zcs.

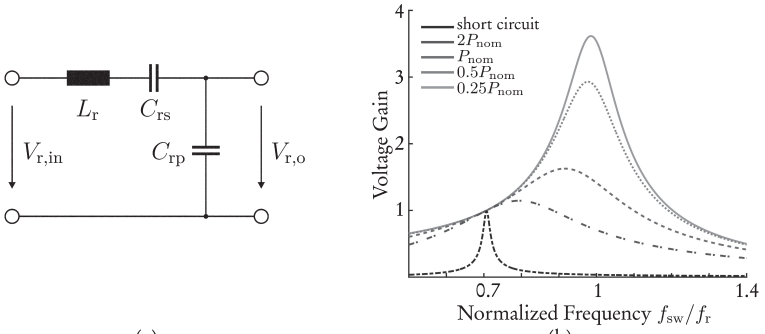


Figure 2.7.: Resonance tank (a) and voltage gain diagram (b) of a LCC series parallel converter

2.2.2. Dual Resonance Circuits

With a third energy storage element added to the system, resonance circuits with two gain peaks can be implemented. One type of three-element converters are series-parallel resonance converters, that add a second eigenfrequency to the network. Two series parallel resonance converters, the LCC and the LLC converter will be discussed in this section. An overview over resonance tank circuits with tree energy storage elements is given in [Bat94].

The LCC network is shown in Figure 2.7 and consists of a series inductance L_r, a series capacitor C_{rs} and a parallel capacitor C_{rp}. The voltage gain function is visualized in part (b) of the figure, and the corresponding equation is

$$G(s) = \frac{s}{L_r C_{rp} s^3 + \frac{L_r}{R_L} s^2 + \left(\frac{C_{rp}}{C_{rs}} + 1\right) s + \frac{1}{R_L C_{rs}}}. \tag{2.7}$$

The network forms a third order bandpass with two eigenfrequencies. At high power the parallel capacitor is shortened by the load and hence, resonance occurs at $f_{r1} = 1/2\pi\sqrt{L_r C_{rs}}$. Like in the SRC, at this point the gain for all load cases is 1. With decreasing load, the influence of the parallel capacitance increases, which causes the resonance to shift to higher frequencies towards $f_r = 1/2\pi\sqrt{L_r \frac{C_{rs} C_{rp}}{C_{rs}+C_{rp}}}$ and – similar to the parallel resonance converter – the height of the gain maximum to increase. In zvs operation, LCC converters are problematic, due to their light load peaks in the frequency range between the zvs high load area and the zvs light load area. If the

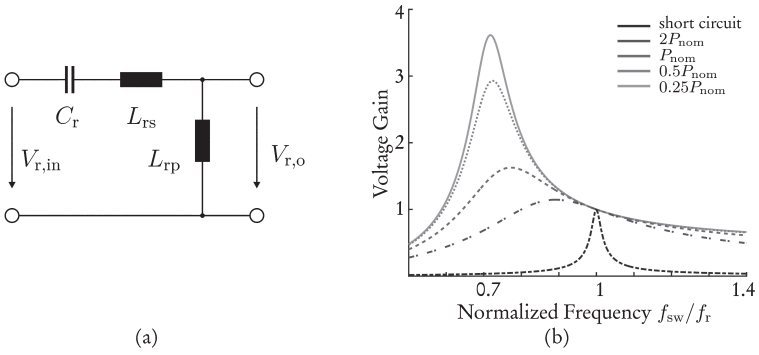


Figure 2.8.: Resonance tank (a) and voltage gain diagram (b) of a LLC series parallel converter

converter load is reduced, the voltage peaks must be overcome to stabilize the output frequency, this can lead to damage on the converter [Yan03].

A second common way to form a series parallel resonance tank is to connect a capacitor C_r and an inductor L_{rs} in series and a second inductance L_{rp} parallel to the load. This LLC topology and its voltage gain curves are depicted in Figure 2.8. The gain function is

$$G(s) = \frac{s^2}{\frac{L_{rs}}{R_L}s^3 + (\frac{L_{rs}}{L_{rp}} + 1)s^2 + \frac{1}{R_L C_r}s + \frac{1}{L_{rp}C_r}}. \tag{2.8}$$

The principles of operation are very similar to the ones of the LCC converter. The difference lies in the order of the resonance frequencies for high and light load. For high load, the parallel inductance is shortened and therefore, the resonance frequency is $f_r = 1/2\pi\sqrt{L_{rs}C_r}$, where the gain for all loads is 1. For light load, resonance shifts towards the lower frequency $f_{r1} = 1/2\pi\sqrt{(L_{rs}+L_{rp})C_r}$. For efficient hardware designs, in converters with a transformer, the magnetizing or transformer main inductance L_M can be used as parallel inductance and the primary leakage L_1 as part of the serial inductance [JK07, Hua10]. The principles of operation of LLC resonance converters will be further detailed in section 2.3.

In dual resonance converters, the steepness of the voltage gain functions and the amplification for certain loads depends on the distance between the two resonance frequencies. For LLC converters, this is quantified by the design parameter normalized

inductance $L_n = {}^{L_M}/_{L_r}$, for small L_n, the resonance frequencies are close together, for large L_n, they are far apart from each other. For small normalized inductances, the maximal achievable gain and the load, for which gains in excess of 1 are achievable, are large, the slopes of the gain function plot are steep. With increasing normalized inductance, the gains decrease and the slopes become more even. [Hua10] The discussed behavior of the converter has consequences for the voltage control. At small normalized inductance, a larger load margin can be stabilized with the same switching frequency range, than in controllers with large L_n.

2.2.3. Triple Resonance Circuits

In [Bat94], all possible combinations for fourth order resonance circuits are given and disused. It is clarified, that not all combinations qualify for resonant converter operation and of those, most are of minor relevance in praxis [Bat94].
Fourth-order resonance circuits are becoming more relevant with increasing operating frequencies, where component parasitics as transformer leakage inductance and winding capacitance, and semiconductor junction capacitances can be utilized to form the resonance circuit. Additionally, the use of parasitics contributes to the converter size and cost reduction. Necessary frequency range to achieve wide load margins further shrinks, compared to second and third order resonance topologies due to the higher filter order. On the other hand, this high order induces high order nonlinearities and hence, the steady state analysis becomes more difficult, but first order harmonic analysis still delivers acceptable results. [Bat94]
Further discussion on LC(T)LC-type converters with LC(T)LC-type converters will not be further considered in this work and are only mentioned the for sake of completeness. Detailed analysis on this converter type is given in [SBD+02] and [DBK12].

2.3. LLC Converters

The LLC resonance converter is a dual resonance peak converter, that combines the behavior of a SRC in high load with that of a PRC in light load. The resonance frequency in the SRC-type behavior is higher than the one of the PRC-type, because the effective inductance of the parallel resonance frequency adds the transformer magnetizing inductance to the serial resonance inductance and hence is always larger than the serial one. This relation and the achievable gains in series and parallel converters result in the LLC-typical gain curve shape. Resonance tank scheme and DC gain curves are given in Figure 2.8b and were briefly discussed under dual resonance

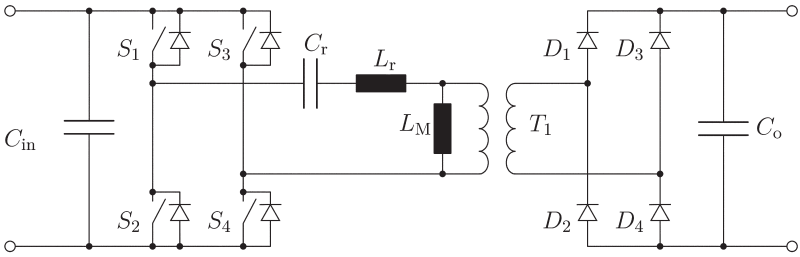


Figure 2.9.: Setup of a LLC resonance converter, with blocking capacitor, inverter with rectangular voltage output, resonance circuit, transformer with depicted magnetizing inductance, inverter and filter capacitor.

converters in subsection 2.2.2. A full scheme of an LLC converter with full bridge inverter and rectifier is given in Figure 2.9. The DC input voltage is inverted to rectangular AC voltage and applied to the resonance circuit, that consists of a capacitor C_r, an inductor L_r in series to the load and – parallel to the load – the transformer magnetizing inductance L_M. The input to output voltage relation is adapted with the transformer T_1, that also realizes galvanic isolation between the converter terminals. The rectifier is depicted as diode full bridge. Capacitors C_in and C_o reduce High Frequency (HF) coupling of the converter to the in- and output DC lines. The inverter can either be a full bridge or a half bridge. The implementation of a full or half bridge has no influence on the principal functionality of the converter, see [AR12, PTB10] and [Yan03, JK07]. However, for given power ratings, quantities like the power factor are different for full and half bridge converters, this will be discussed in section 2.3.2. For the output, full wave rectifiers, ether full bridges or transformers with center tap on the secondary, are common. In the following, the fundamentals of this converter type will be detailed.

LLC converters meet most of today's requirements for power converters in high power applications (see section 1.2), as good controllability of the output voltage and compact designs. High efficiency is gained by resonant operation, that can be achieved over a wide load range. Due to its DC gain character from Figure 2.8b, buck-boost type converters can be implemented [JK07]. The bandwidth of the operating frequency can be small, even if a broad load range is to be covered, therefore gain adjustments are executed by narrow frequency changes and hence ensure high converter dynamics. The operating area is completely on the negative slope, the gain maximum does not need to be overridden for means of regulation. The integration of the resonance inductance and the transformer into one device can further reduce the converter size [Yan03, Hua10] Secondary side rectifier diodes are commutated at zero current,

which is favorable with respect to efficiency and component stress [JK07]. Due to the second order low pass characteristics of the resonance circuit, high frequency signal components of the square wave input voltage are suppressed, component stress and EMI is reduced. [Yan03, JK07, Hua10]

2.3.1. Operation Principles of LLC Converters

Generally, LLC converters are designed to operate on the negative slope of the voltage gain diagram in zvs mode of the inverter semiconductor switches. The voltage stabilization is ensured by adaption of the input inverter's switching frequency in the resonance frequency's vicinity.

The converters operation mode can be distinguished by operation at, below and above resonance frequency. The corresponding waveforms are given in Figure 2.10, showing the on-states of the switches $S_1 \dots S_4$, the resonance current i_r with the transformer magnetizing current i_M and the AC secondary side current i_sec with the diodes, where it runs through, from top to bottom. Note that the current in the resonance tank is the sum of the magnetizing current and the current, taking part in the power transfer, to the secondary side. The qualitative waveform is equal for converters with full- or half bridge inverter – see e.g., [JK07] and [PTB10]. In a full bridge setup, energy is delivery from the DC input to the resonance circuit every half cycle. In a half bridge configuration, the energy for one full cycle is obtained from the DC side in the first half cycle. In the second half cycle, the resonance circuit is shortened by the semiconductor switch S_2, that causes the primary current to circulates within the resonance circuit and energy, stored therein, is transferred to the output. [Yan03, JK07, Hua10]

Figure 2.10a gives the converters waveforms at f_r. The switching cycle starts at t_1 when the switches S_1 and S_4 are open. Precisely this is the instant, when the falling current in the resonance tank reaches the value of the magnetizing current. The opening of the switches forces the transformer magnetizing current to commutate to the antiparallel diodes of the opposite switches, which are still open. With the current in the antiparallel diodes, the voltage drops across switches S_2 and S_3 is as low as the diode forward voltage V_df, and hence, quasi zvs can be achieved. The magnetizing current does not contribute to the energy transfer. Consequently, when the primary current falls to the value of i_M, the current of the secondary side diodes reaches zero, power transfer is stopped. In the consequence turn of under zero current condition is achieved for the secondary diodes. [JK07]
When S_2 and S_3 are closed after a small dead time at time instance t_2, the current quickly falls to zero and commutates from the diodes to the now closed switches. At

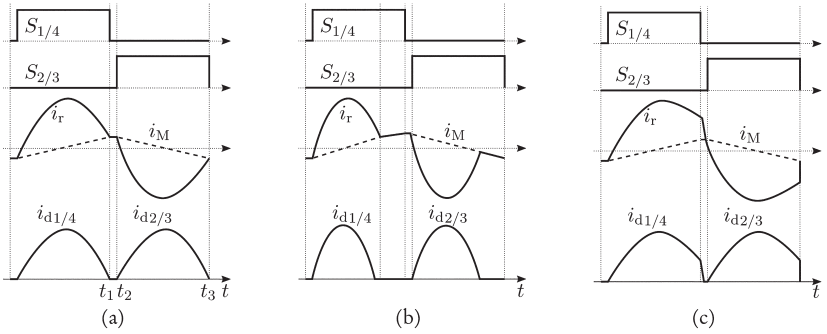


Figure 2.10.: Typical current waveforms of a LLC full bridge converters (a) at, (b) below and (c) above resonance frequency f_r.

the same time, the magnetizing current is reversed and begins to fall. In the time interval t_2 – t_3, the resonance current describes a negative half wave, that has the form of the sum of a sinusoidal half wave and a ramp, where the ramp is the part of the magnetizing current, falling linearly over the complete interval. In a converter with full bridge inverter, the resonance circuit is connected to the DC input by the closed switches and energy flows into the circuit. With a half bridge inverter, in this interval, the resonance circuit is shorted and energy from the foregoing half wave circulates in the circuit. At instance t_3, the resonance current has reached the value of the magnetizing current and S_2 and S_3 are opened and energy transfer is stopped. During the complete interval, energy is transferred to the secondary side and the secondary current describes a quasi-sinusoidal half wave. [JK07]
With the commutation of the magnetizing current to the antiparallel diodes of S_1 and S_4, the positive half cycle begins, the waveforms of the first half-cycle are repeated with inverted sign. In the positive half cycle, the full and half bridge inverter both connect the resonance circuit to the DC supply and energy flows into the converter. The secondary current is only shortly interrupted during the dead time between t_1 and t_2 and an optimum between soft commutation of the secondary diodes and acceptable ripple. [JK07]

The waveforms for the operation area, where the slope of the DC gain curve is still negative and the switching frequency is below f_r, are given in Figure 2.10b. In this mode, the quasi-sinusoidal current half wave duration is shorter than the on-time of the conducting path. Most of the statements from the previous paragraph for operation at resonance frequency are still valid. When the resonating part of the current reaches the value of the magnetizing current, energy transfer is stopped, thus the secondary

current reaches and will remain zero until the beginning of the following half cycle. In the resonance circuit the magnetizing current continues to flow, until the inverter switches are turned off and commutation begins. [JK07]
On the primary side, the switches are turned on under zvs condition, the turnoff is executed with switch current reduced to the magnetizing current. The secondary side commutation condition equals the one at resonance frequency. Due to the interrupted secondary current, the current-time integral is reduced. Therefore, the current peak and hence the losses namely in the semiconductors rise to transmit the same amount of energy at the same voltage levels as at f_r. [JK07]

The third operation region lies above f_r, the corresponding waveforms are given in part (c) of the figure. Here, the conducting path is interrupted, before the resonance current has fallen to the value of the magnetizing current. At turn-off, the current is forced to rapidly fall to zero and commutate to the antiparallel diodes of the opposite current branches. The turn-on of the switches for the next half cycle path is executed, while the falling current still flows through the diode to ensure zvs in this mode. The short on-time of the primary side switches results in a loss of zcs for the secondary diodes (see figure). [JK07]
The higher primary turn-off current and the loss of zcs for the secondary diodes causes increased converter losses in this operating mode.

2.3.2. First Harmonic Approximation

For the purpose of converter design, a mathematical model with good computational qualities is useful. Therefore, the converters input voltage square wave is approximated by its sinusoidal fundamental. In the case of second order resonance converters, the method of First Harmonic Approximation (FHA) leads to sufficiently good results for design purposes, since only quasi sinusoidal currents occur in the converter and only the input voltages fundamental contributes to the power transfer [JK07].

Limitations are clearly given in the converters dynamic transfer behavior coming from the absence of the blocking and filter capacitors in the model.

In literature, e.g., [Yan03, JK07, LL10], the circuit from Figure 2.9 is commonly simplified as given in Figure 2.11 by neglection of ohmic losses, the transformer stray inductances and internal voltage drops and losses in the inverter and rectifier. In Subfigure (a), the inverter is represented by a square wave voltage source with effective voltage V_in. The transformer secondary side and connected components are transformed to the primary. The load is represented by an ohmic resistance, its primary side equivalent is R'_L. For the FHA the equivalent circuit from Subfigure

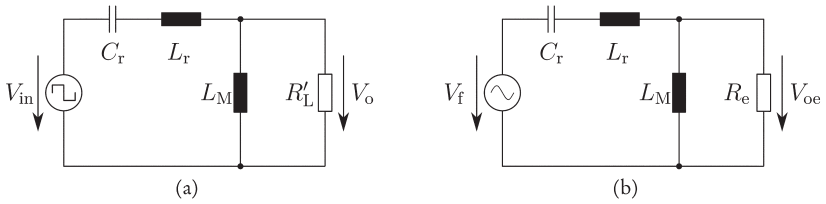


Figure 2.11.: For FHA simplified equivalent circuit of an LLC resonance converter with rectangular (a) and sinusoidal (b) excitation, as commonly used in literature e.g., [Due98, JK07]

2.11b is introduced, where the square wave voltage source is replaced by the sinusoidal voltage V_f and R'_L by R_e, where the equivalent sinusoidal voltage V_{oe} drops. Here, the input Root Mean Square (RMS) voltage

$$V_f = \frac{2\sqrt{2}}{\pi} V_{in} \tag{2.9}$$

is the first coefficient of the Fourier series of the rectangular oscillation V_{in} and

$$V_{oe} = \frac{2\sqrt{2}}{\pi} n V_o \tag{2.10}$$

is the transformed fundamental of the output voltage V_o, where n is the transformer turns ratio or respectively the corrected turns ratio. The equivalent output current

$$I_{oe} = \frac{\pi}{2\sqrt{2}} \frac{1}{n} I_o \tag{2.11}$$

flow through R_e, I_o is the converter DC output current. The equivalent load resistance is the ratio of equivalent output voltage to current and hence, is defined

$$R_e = \frac{V_{oe}}{I_{oe}} = \frac{8n^2}{\pi^2} \frac{V_o}{I_o} = \frac{8n^2}{\pi^2} R_L, \tag{2.12}$$

where R_L is the DC load equivalent resistance. In the equivalent circuit, the transformer magnetizing inductance is parallel to R_e and hence, V_{oe} is applied to it. Therefore, the magnetizing current is

$$I_M = \frac{1}{j\omega L_M} V_{oe} \tag{2.13}$$

with the angular frequency

$$\omega = 2\pi f_{\mathrm{sw}}, \tag{2.14}$$

where f_{sw} is the operating frequency of the converters input inverter.

The goal of the FHA model is to derive a DC input to output voltage gain function. Thus, the network of the equivalent circuit is described by its nodal- and mesh equations. For complex networks systematic methods like the method of the complementary tree should be applied [FLM05]. With the given circuit diagram and the relations above, the problem at hand can be analyzed straight forward. The outer mesh yields

$$V_{\mathrm{f}} = \left(\mathrm{j}\omega L_{\mathrm{r}} + \frac{1}{\mathrm{j}\omega C_{\mathrm{r}}}\right) i_{\mathrm{r}} + V_{\mathrm{oe}}. \tag{2.15}$$

The left mesh confirms, that V_{oe} applies to R_{e} and L_{M} as

$$V_{\mathrm{oe}} = \mathrm{j}\omega L_{\mathrm{M}} I_{\mathrm{M}} = R_{\mathrm{e}} I_{\mathrm{oe}} \tag{2.16}$$

and hence, the output current can be solved to

$$I_{\mathrm{oe}} = \mathrm{j}\omega \frac{L_{\mathrm{M}}}{R_{\mathrm{e}}} I_{\mathrm{M}}. \tag{2.17}$$

The networks node yields

$$i_{\mathrm{r}} = I_{\mathrm{M}} + I_{\mathrm{oe}} = \left(1 + \mathrm{j}\omega \frac{L_{\mathrm{M}}}{R_{\mathrm{e}}}\right) I_{\mathrm{M}}, \tag{2.18}$$

that is inserted into equation (2.15), with (2.15), yielding

$$V_{\mathrm{f}} = \left(\mathrm{j}\omega \frac{L_{\mathrm{r}}}{R_{\mathrm{e}}} + \frac{L_{\mathrm{r}}}{L_{\mathrm{M}}} + 1 + \frac{1}{\mathrm{j}\omega R_{\mathrm{e}} C_{\mathrm{r}}} + \frac{1}{(\mathrm{j}\omega)^2 C_{\mathrm{r}} L_{\mathrm{M}}}\right) V_{\mathrm{oe}}, \tag{2.19}$$

$$\frac{V_{\mathrm{oe}}}{V_{\mathrm{f}}} = \frac{(\mathrm{j}\omega)^2 R_{\mathrm{e}} C_{\mathrm{r}} L_{\mathrm{M}}}{(\mathrm{j}\omega)^3 C_{\mathrm{r}} L_{\mathrm{r}} L_{\mathrm{M}} + (\mathrm{j}\omega)^2 R_{\mathrm{e}} C_{\mathrm{r}} (L_{\mathrm{r}} + L_{\mathrm{M}}) + \mathrm{j}\omega L_{\mathrm{M}} + R_{\mathrm{e}}}, \tag{2.20}$$

which is the complex transfer function of the equivalent circuit in Figure 2.11b.

In the state-of-the-art resonant converter modeling, the voltage gain function is normalized to the resonance frequency. Therefore, the normalized switching frequency

$$f_\mathrm{n} = \frac{f_\mathrm{sw}}{f_\mathrm{r}} \tag{2.21}$$

relates the inverter frequency to the circuits full load resonance frequency and hence, the resonance is at unity. The inductance

$$L_\mathrm{n} = \frac{L_\mathrm{M}}{L_\mathrm{r}} \tag{2.22}$$

gives the ratio of resonance to transformer magnetizing inductance. In [PTB10], the quotient of the effective inductances in full and light load is defined as

$$\sigma = \frac{L_\mathrm{r}}{L_\mathrm{r} + L_\mathrm{M}} = \frac{1 + 1/L_\mathrm{n}}{1/L_\mathrm{n}}. \tag{2.23}$$

With the given substitutions and the quality factor

$$Q_\mathrm{e} = \frac{1}{R_\mathrm{e}} \sqrt{\frac{L_\mathrm{r}}{C_\mathrm{r}}}, \tag{2.24}$$

the converter gain characteristic can be expressed in a form, where it is normalized versus the resonance frequency. Consequently, the absolute value of the converters FHAs input to output voltage gain (2.20) is formed, and the circuit parameters are substituted by the above given relations, yielding

$$M_\mathrm{fha} = \left| \frac{V_\mathrm{oe}}{V_\mathrm{f}} \right| = \frac{f_\mathrm{n}^2 \omega_\mathrm{r}^2 R_\mathrm{e} C_\mathrm{r} L_\mathrm{M}}{\sqrt{\left(R_\mathrm{e} - f_\mathrm{n}^2 \omega_\mathrm{r}^2 R_\mathrm{e} C_\mathrm{r} \left(L_\mathrm{r} + L_\mathrm{M}\right)\right)^2 + \left(f_\mathrm{n} \omega_\mathrm{r} L_\mathrm{M} - f_\mathrm{n}^3 \omega_\mathrm{r}^3 C_\mathrm{r} L_\mathrm{r} L_\mathrm{M}\right)^2}} \tag{2.25}$$

$$= \frac{f_\mathrm{n}^2}{\sqrt{\left(f_\mathrm{n}^2 - \sigma\right)^2 \left(1 + 1/L_\mathrm{n}\right)^2 + Q_\mathrm{e}^2 \left(f_\mathrm{n} - f_\mathrm{n}^3\right)^2}} \tag{2.26}$$

for the FHA models stationary converter gain, where L_n is the normalized inductance (see equation (2.22)). With the given gain function, the expected load and frequency dependent voltage drop across a connected load R_L at the output of an LLC converter can be approximated. The voltage excitation for exact results with the gain function (2.26) is the sinusoidal first harmonic of the according rectangular LLC converter AC excitation, it is injected at the AC input of the converters resonance circuit. The fictional converter equivalent load R'_L for this approximation is directly connected, in

parallel, to the converter's transformer magnetizing inductance L_{M} and experiences AC voltage drop across it. Based on the above taken assumptions, the FHA model is a good reflection of the LLC converter and the relation

$$M_{\mathrm{fha}} \approx M_{\mathrm{DC}} = \left| \frac{nV_{\mathrm{o}}}{V_{\mathrm{in}}} \right|, \tag{2.27}$$

between M_{fha} and the stationary, normalized converter DC gain M_{DC} holds true. The right side of this equation represents the converter gain from its DC input to its primary side transformed DC output. This relation includes all voltage losses on the converter's inverter and rectifier as well as the resonance circuit excitation by a rectangular waveform. As described further above in this Subsection, the FHA gain function M_{fha} presents a good approximation of LLC converters input to output DC gain characteristics. Additionally, the transformer turns ratio n is compensated in the voltage gain function. [PTB10]

With the model at hand, the DC characteristics of an LLC converter can be determined and different design drafts can be compared. Alongside, the possible gains for specific loads end frequency ranges, the zvs and zcs area can be outlined. DC capacitors cannot be modeled in the given pure AC model, so that they must be neglected. But the dimensioning of the output filter capacitor C_{o} especially influences the transient output voltage behavior and therefore cannot be neglected for dynamic analysis and control tasks. That is why the FHA model is limited to stationary system analysis.

2.4. Control Techniques for DC / DC Converters

To generate and stabilize DC voltage on DC/DC converters output terminals, a voltage controller is mandatory. The primary control objectives are the general criteria control accuracy, achievement of the required system dynamics and error compensation, that are widely discussed in literature, e.g., in [Lun14]. For DC/DC converters, this is voltage stabilization under a certain accuracy, compensation of disturbances of load and input voltage variation. In addition to the voltage control, output current mode control has been established, where the output voltage is indirectly controlled by control of the output current [VSR13]. When turned on, the controller could perform a start-up routine to guarantee, that the required voltage stabilization and/or power provision are met within a defined time limit. For the control signal, the PWM duty cycle of one or more semiconductor switches are commonly used. However, for phase shift converters, the control signal represents the phase between the inverter's half

waves and multi-resonant converters are controlled by the fundamental frequency in the resonance tank.

Subsequent to the primary control objectives, secondary control functions – mainly safety functions – are regularly integrated into the controller structure. Common functions are over current and temperature protection, since both phenomena quickly lead to converter damage. Depending on the application scenario of the converter, safety function can also protect auxiliary equipment such as batteries, by protection from under voltage on the converter primary side.

A basic output voltage controller is a single loop voltage controller. Therefore, the control error is generated by subtraction of the measured converter output voltage from a reference value. The error signal is fed to a controller, which could be a simple compensator or a Proportional-Integral-Derivative (PID) controller. In a PWM converter, the controller output is compared against a sawtooth wave with the converter's specified PWM frequency. The comparator's output is a PWM drive signal for the converter's semiconductor switch, its duty cycle depends on the controller output signal. To avoid instability, the controller response time must be significantly longer than the PWM cycle time. [VSR13]
Such a single loop voltage controller can be extended to a cascaded structure with an underlaid current control loop. Therefore, the sawtooth wave reference is replaced by the measured main inductor current of the converter. The voltage controller output is the inductor current reference signal, hence, the controller parameter set differs from that of the single loop voltage controller. To ensure the desired fixed PWM frequency, an RS latch is connected to the comparator (R) and an external clock to (S). The insertion of the current control loop improves the controller's response time and system stability. Overcurrent protection can be easily implemented by limitation of the current reference signal. Therefore, sub harmonic oscillations may occur. [VSR13]

The application of sliding mode control strategies on power converters is often discussed in literature, e.g., [VSR13, WXC15]. Sliding mode control is a nonlinear controller type for variable structured systems. In the converter's state space, a (hyper) surface is defined and a control law is formalized in a way that the system state variables are steered towards this plane. Once on the plane, the states slide over it towards the system's equilibrium point. The sliding process is a repeated switching back and forth between the half spaces divided by the sliding surface, rather than smooth sliding. This controller type leads to highly robust control loops with short dynamic response times. They maintain good stability for large variation of input voltage and converter load. The complexity grade of their implementation is rather low. On the downside, the controller switching frequency becomes inconstant, which is often undesired

and controller design cannot be based on a systematic design process, like linear PID controllers. [VSR13]

Model Predictive Control (MPC) is a control method, where a mathematical, dynamical model of the system to be controlled is explicitly utilized to compute an optimal control signal for the desired system behavior. The models can be expressed as step response or state-space models [SEMR+15], transfer functions or others. Constraints as input, output and state limitations or time penalties can be integrated straight forward into the model and hence, can be considered in the process of the control signal acquisition. The control signals are computed by predicting the output signal over a given horizon and an optimal control signal is gained by minimizing an objective function. In the subsequent iteration, the prediction horizon is resided for one instance and the control signal is recomputed. For linear models without constraints, and quadratic objective functions, analytic control laws can be obtained, for all other circumstances, control signals have to be computed in an iterative process. [CB07]
MPC is increasingly used by the industry, primarily in the process and chemical sector, where it has reached the state of a quasi-standard. In aerospace and automotive control systems, the number of MPC controllers is significantly increasing.[CB07, PDA15] Power electronic applications feature higher dynamics, than the aforementioned systems, and hence, the implementation of MPC is less common. Nevertheless, MPC implementations in power converters for energy applications or motor drives are reported. These are mainly of academic nature, but industrial applications are also known. [PDA15, SEMR+15] MPC feature good control performance, including high dynamic, good control error and disturbance compensation. Therefore, MPC requires high design effort and the knowledge of precise system models. For the real time execution of most MPC algorithms, high computational power is required.

2.4.1. Trajectory Planning and Tracking for State Transitions

In situations like the startup or the shutdown of a DC/DC converter, the converter output is in a transient operating state. Often primarily the finite state is of interest, while the starting point is given by the steady state of the system before the transition. By implementing such a transition by a step of the reference signal, violation of control quality criteria, such as exceeding maximum values and hence, risking system destruction is the consequence. Alternatively, the reference signal can be shaped in a way, that the system output can track it exactly. Therefore, a reference trajectory with given values at given time instances is computed, steering the system from one output state to another. According to [Lun14, Ch. 7], for a system with continuously

differentiable input to output relation and relative grade $r = n - q$, an error free traceable trajectory $w(t)$ for an output transition is described by a polynomial of grade $p = 2r + 1$,

$$w(t) = a_{\mathrm{w}p}t^p + \cdots + a_{\mathrm{w}1}t + a_{\mathrm{w}0}, \tag{2.28}$$

where r is the relative grade of the system. The following set of p linear equations is formed by the given polynomial (2.28), its r first derivations and the output transitions constraints for the start- and end-time $t = 0$ and $t = t_\mathrm{e}$, respectively:

$$y(0) = w(0) = \bar{w}_0 \tag{2.29}$$

$$y^{(i)}(0) = w^{(i)}(0) = 0, \qquad i = 1, 2, \ldots, r \tag{2.30}$$

$$y(t_\mathrm{e}) = w(t_\mathrm{e}) = \bar{w}_\mathrm{e} \tag{2.31}$$

$$y^{(i)}(t_\mathrm{e}) = y^{(i)}(t_\mathrm{e}) = 0, \qquad i = 1, 2, \ldots, r. \tag{2.32}$$

At the start and end of the transition, the system output is aimed to be in a stationary state, and hence, the derivatives vanish in 0 and t_e, respectively. The output value before the start of the transition is $\bar{w}_0$ and the system is generally asumed to be in stationary state. After the end of the transition, the system should remain at the target value for the end of the transition $\bar{w}_\mathrm{e}$ infinitely:

$$y(t) = \bar{w}_\mathrm{e}, \qquad \forall\, t \geq t_\mathrm{e}. \tag{2.33}$$

By solving the linear system, a trajectory to transfer the system output from one value to a new one is given. The system will be capable to track the trajectory without control error. [Lun14, Ch. 7]

One option to compute a control signal from a given output trajectory $w(t)$ makes use of the input-output normal form [Lun14, Ch. 7]. This form in the state space differs the system dynamics into the zero dynamics and the internal dynamics [Lun14, Ch. 5]. This leads to the control law

$$\Sigma_\mathrm{V} : \begin{cases} \dot{\boldsymbol{x}}_\mathrm{N}(t) &= \boldsymbol{A}_\mathrm{NN}\boldsymbol{x}_\mathrm{N}(t) + \boldsymbol{b}_\mathrm{N}w(t), \qquad \boldsymbol{x}_\mathrm{N}(0) = \boldsymbol{x}_\mathrm{N0} \\ u(t) &= -\boldsymbol{c}_\mathrm{N}^\mathrm{T}\boldsymbol{x}_\mathrm{N}(t) - \boldsymbol{v}^\mathrm{T}\boldsymbol{x}_\mathrm{I,ref}(t) \end{cases}. \tag{2.34}$$

where the output is the control signal. It is computed by the systems reference internal dynamics

$$\boldsymbol{x}_{\mathrm{I,ref}} = \begin{pmatrix} w(t) \\ w^{(1)}(t) \\ \vdots \\ w^{(r)}(t) \end{pmatrix}, \tag{2.35}$$

that are the output trajectory and its r first deviations and the zero dynamics $\boldsymbol{x}_{\mathrm{N}}$, that is computed from the internal $\boldsymbol{A}_{\mathrm{NN}}$ matrix and the reference trajectory. [Lun14, Ch. 7] The state matrices, input and output vectors for the input output normal form can be gained by the state space transformation as described in [Lun14, Ch. 5.].

2.5. Fundamentals of Switched Systems

Some dynamic systems include properties, that lead to discrete state transitions in an otherwise continuous dynamic behavior. Discrete transitions are typically based on physical effects, such as closing/opening a hydraulic valve or the operation of a (semiconductor-) switch in an electronic circuit. Such systems are described in literature as *switched systems*

$$\dot{\boldsymbol{x}} = \boldsymbol{f}_{\sigma(t)}(\boldsymbol{x}(t), u(t)), \tag{2.36}$$

where the vector field $\boldsymbol{f} \in \mathbb{R}^n$ describes the state $\boldsymbol{x} \in \mathbb{R}^n$ and input $u \in \mathbb{R}$ dependent state dynamics. With a discrete state transition, one state function is replaced by the state function representing the new system dynamics. This is indicated in (2.36) by the switching rule index $\sigma(t) \in \mathbb{M}$, which is also the switching rule function, that determines the active state function and $\mathbb{M} \in \mathbb{R}$ is the set of valid solutions for $\sigma(t)$. [Goe12] [SG05]

The superordinate class of switched systems is sub organized in classes by their type of switching behavior, for example in *state-dependent* versus *time-dependent* switching. In time dependent switching the switching solely follows a given time pattern, whereas state dependent switching events take place, when system states fulfill certain conditions. Switched systems can exist as *controlled* switched systems or in form of *autonomous* switched systems, where the input u in equation (2.36) vanishes. If the switching behavior is considered *arbitrary*, the switching behavior is not further constrained. System statements as stability, made on arbitrary switching systems hold true for all sub classes, hence analysis methods for arbitrary switching

systems can be applied to any sub class of switching systems. For the problem at hand, properties of continuous time switched linear systems will be reviewed more closely and stability analysis methods for these systems will be presented.

2.5.1. Continuous Time Switched Linear Systems

If the continuous part of the switched system only contains linear correlations in all subsystems, the problem becomes a *continuous time switched linear system*. The state equation for the single input-controlled system version can then be written – similar to the Linear Time-Invariant (LTI) form – as

$$\dot{\boldsymbol{x}}(t) = \boldsymbol{A}_{\sigma(t)}\boldsymbol{x}(t) + \boldsymbol{b}u(t), \tag{2.37}$$

where $\boldsymbol{A}_{\sigma(t)} \in \mathbb{R}^{n\times n}$ is the set of state matrices and $\boldsymbol{b} \in \mathbb{R}^n$ is the input vector. With every switching event, the system matrix $\boldsymbol{A}_{\sigma(t)}$ changes from one index to another and therewith performs the switching event. [SG05, Ch. 1]

2.5.2. Stability Analysis of Switched Linear Systems

Stability analysis of switched linear systems addresses the problem, under which conditions the switched linear system (2.37) is asymptotically stable. The solutions for systems under arbitrary switching are valid for any admissible sets of $\sigma(t)$. If a system is unconditioned stable, then it is globally (asymptotically) stable.

According e.g., to [SG05, Ch. 2], [Goe12], stability of a switched linear system is given, if the following definitions hold true. For simplicity, let's assume the systems equilibrium point is the origin $\boldsymbol{x}_\mathrm{e} = 0$, without loss of generality. Then, $\boldsymbol{x}_\mathrm{e}$ is Lyapunov-stable, if for all $\epsilon > 0$ there exists a $\delta > 0$ such that

$$\|\boldsymbol{x}(t_0)\| \leq \delta \quad \Rightarrow \quad \|\boldsymbol{x}(t)\| \leq \epsilon \quad \forall\, t \geq 0. \tag{2.38}$$

If (2.37) fulfills (2.38) and furthermore, a δ exists, such that

$$\|\boldsymbol{x}(t_0)\| \leq \delta \quad \Rightarrow \quad \boldsymbol{x}(t) \to 0 \quad \text{for} \quad t \to \infty, \tag{2.39}$$

then, the system is asymptotically stable. The entirety of all δ, for which (2.39) holds true is denoted as the region of attraction. If, for the region of attraction $\delta\ \forall\ \mathbb{R}^n$ holds true, the system is globally asymptotically stable.

The above given definitions cannot be practically applied to a system under examination for proof of stability, due to an infinite set of candidate solutions. One way to practically investigate systems stability is Lyapunov's direct method. For Lyapunov's direct method, a function $V(\boldsymbol{x})$ is defined, that is positive definite and real, continuously differentiable for all $\boldsymbol{x} \in \mathbb{D}^n \subseteq \mathbb{R}^n$, with

$$\dot{V}(\boldsymbol{x}) \leq 0 \quad \forall\, \boldsymbol{x} \in \mathbb{D}^n \subseteq \mathbb{R}^n, \tag{2.40}$$

then, it is a Lyapunov function to the vector field $\boldsymbol{x}$ in the area $\mathbb{D}^n$. The equilibrium point with $\dot{\boldsymbol{x}}_\mathrm{e} = 0$ is stable, if

$$\dot{V}(\boldsymbol{x}) \leq 0 \quad \forall\, \boldsymbol{x} \in \mathbb{D}^n, \tag{2.41}$$

asymptotically stable if

$$\dot{V}(\boldsymbol{x}) < 0 \quad \forall\, \boldsymbol{x} \neq \boldsymbol{x}_\mathrm{e} \tag{2.42}$$

and globally stable or globally asymptotically stable, if $\mathbb{D}^n = \mathbb{R}^n$ in (2.41) or (2.42), respectively.

From a strict standpoint, in the above given statements, one would need to consider the definitions and criteria for time-varying systems as given in [Vid02, Ch. 5]. This will not be further detailed in this thesis for conciseness reasons.

For verification of stability, Lyapunov's direct method is applied on an autonomous LTI system

$$\boldsymbol{A}\boldsymbol{x} = \dot{\boldsymbol{x}} \tag{2.43}$$

and an arbitrary positive definite symmetric matrix $\boldsymbol{Q}$. Therefore, a positive definite symmetric matrix $\boldsymbol{P}$ is to be found to satisfy the Lyapunov equation

$$\boldsymbol{A}^T\boldsymbol{P} + \boldsymbol{P}\boldsymbol{A} = -\boldsymbol{Q}. \tag{2.44}$$

Then, the Common Quadratic Lyapunov Function (CQLF)

$$V(\boldsymbol{x}) = \boldsymbol{x}^T\boldsymbol{P}\boldsymbol{x} \tag{2.45}$$

and its derivation

$$\dot{V}(\boldsymbol{x}) = -\boldsymbol{x}^T\boldsymbol{Q}\boldsymbol{x} \tag{2.46}$$

are defined. [SG05, Ch. 2]

For switched linear systems with switched state matrices $\boldsymbol{A}_{\sigma(t)}$, the CQLF (2.44) is extended by the switched state matrices to

$$\boldsymbol{A}_\sigma^T \boldsymbol{P} + \boldsymbol{P}\boldsymbol{A}_\sigma < 0 \quad \forall\, \sigma \in \mathbb{M}, \tag{2.47}$$

resulting in the CQLF for switched linear systems. If a certain CQLF can be found with any $\sigma \in \mathbb{M}$ for the problem at hand, global asymptotical stability with arbitrary switching is proven. On the other hand, if no CQLF is found, the system under test is not necessarily unstable – another non-CQLF common Lyapunov function might still be found and stability be proven.

2.6. Contribution to the State-of-Science

The thesis at hand contributes to the state-of-science by putting the high-voltage DC/DC-converter concept as sketched out by Reinold in his patent [Rei02] to an application for tethered mobile machinery with high power and/or large ratio of action. The cited patent describes a DC/DC-converter architecture, where the utilization of low-voltage semiconductor switches are made possible in systems with higher voltage than the semiconductor's blocking voltage capability by a modular converter concept. By this, Reinold states, a low-cost and flexible HV DC/DC converter is achieved. In his patent, Reinold proposes this converter architecture for use in HVDC transmission systems to branch from one transmission line to another or to directly feed from a lower DC voltage (e.g., from photovoltaik) to a transmission line.
In this thesis, the modular concept is picked up and combined with the LLC converter type for the modules. Since the target application's voltage is lower and hence the module voltage becomes lower, advantages as good controllability and fast-switching capability of LV semiconductors can be exploited in the application. This concept allows the new application of such converters to tethered mobile machines, so that high DC voltage from the tethering line can be converted to LV machine voltage (e.g., 800 V) in a compact and efficient manner.

To the best of the author's knowledge and belief, up to the present, there exists no literature addressing the topic of control synthetization of voltage controllers for frequency-driven power converters, such as LLC converters. With this thesis, this topic is firstly addressed. In preparation for the controller synthetization, the LLC converter is modeled in the switched linear LTI domain and analyzed for stability for the first time. Based on the analysis' conclusions, a control law for the LLC converter and the modular HV DC/DC converter is presented.

3. Modular High Voltage DC / DC Power Converter

High voltage DC/DC converters are power converters, that feature at least one high voltage terminal, which can be ether the input, the output or both terminals, if the converter is applied to interconnect two high voltage systems. A modular DC/DC converter in the background of this work implies the existence of a number of similar power stages, i.e., key parameters sum up to the overall converter parameters. The number of modules in one converter is variable. If a high voltage DC/DC converter features a modular structure in accordance with the above definition, it is a *Modular High Voltage DC/DC Converter*.

Currently, high DC voltage is mainly utilized for electrical energy distribution, e.g., to interconnect AC grids or to connect remote power plants, such as offshore wind farms. The electrical power of the wind turbines is collected in a local AC grid, AC/DC converted and transmitted via HVDC transmission line to shore. The local AC structure on the wind farm is fed from the DC links of the turbines by inverters. In a future setup, the local AC structure could be eliminated and replaced by a DC system, where the turbines are connected to the transmission line by DC/DC converters connected together. Such a scenario is discussed e.g., in [MP15]. A second application field not yet exploited in practice, but can be worthwhile, is the supply of high power tethered mobile machines with electrical power. State-of-the-art tethered mobile machinery is powered at low voltage – measured on the transmitted power, which leads to low power density systems with limited ratio of action. Both applications are discussed in the introduction and will be detailed at the end of this Chapter.

The converter to be designed, should be suitable for various application fields, including mobile machinery, therefore, the following requirements to the converter hardware must be met. The voltage and power ratings and conversation ratio should be flexible. With respect to mobile or other applications, where space and weight are critical, the converter should feature high volumetric and gravitational power density. For the high power-density, but also for economical operation, losses should be kept low. In certain scenarios, electrical sub-circuits must be galvanically isolated, hence, galvanic isolation from the primary to the secondary side is required for the converter.

In the following sections, a concept for a high voltage DC/DC converter based on a flexible, modular structure is presented and the design of the modules is detailed. This is followed by two application scenarios for high voltage DC/DC converters, that present the major research motivation of the given project.

3.1. Conception of a DC / DC Converter for High Voltage

The objective of a DC/DC converter for high voltage application is a compact and efficient power converter that is capable to operate in the voltage domain well above 1 kV. The converter aimed for utilization in various fields of application, such as offshore wind farm DC grid connection, or tethered mobile machines. Within those fields the power demands may vary, i.e., from machine to machine, hence scalability is a favorable converter feature. Converter qualities, needed to meet the applications demands as semiconductor blocking voltage and volume reduction are discussed and a concept for a suitable converter is given.

The achievable power density of voltage converters depends on a number of different factors, that were described in detail in Chapter 2. The first is the operating frequency of the converter's AC components, with increasing frequency, transformers and other passive components become less bulky. Especially in low frequency systems, these parts heavily contribute to the total mass and volume, and hence increasing the operating frequency offers large potential to improve the power density. The increasement of the operating frequency is limited by rising switching losses, that need to be dissipated, which leads to the next factor; the efficiency of the converter. With higher losses, the surfaces, must be increased and from a certain point, additional active cooling equipment is required, contributing additional weight and volume. A small contribution to the achievable power density of electronic devices comes from the occurring voltages and hence the growing isolation thicknesses with increasing voltage.

The major design challenge for high voltage DC/DC converters was discussed in Section 1.1, which is to unite the required high blocking voltage for the converter's semiconductors with the demanded compact converter design. MOSFETs and IGBTs for such high frequencies, as they would be required for compact designs, feature only low blocking voltages. IGBTs exist for higher blocking voltages than MOSFETs, but the maximal possible switching frequency decreases with increasing voltage and the voltage limit is still low, compared to semiconductor switches, such as Thyristors. To handle higher voltages, in AC/DC and DC/AC converters, topologies, as flying

capacitor, diode clamped or multilevel topologies represent the state-of-the-art. With these circuits, the maximal converter terminal voltage can be increased over the blocking voltage of a single semiconductor switch by distributing it to a number of switches. To use such inverters / rectifiers for high voltage DC/DC converters, a resonance circuit with a transformer needs to be added and be operated at maximally possible frequency. Therefore, the inverters AC terminal is to be operated at high voltage in the kHz range and the series semiconductor switches are to be operated at zcs and/or zvs. This seems an appropriate topology for a HV DC/DC converter but the synchronous switching of a large number bears some uncertainties, also this converter would lag of modularity, due to the transformer.

A second voltage converter topology, where high voltage is distributed to a number of semiconductor switches has been published under the term of *Medium Frequency Transformer*, e.g., in [SR07, MLC+08]. This converter type is aimed mainly for railway traction applications with one-phase high voltage AC source, mayor design motivation was to reduce space and weight of the transformer on trains. The one-phase high voltage AC input voltage is fed through a number of series connected active full bridge rectifiers. From the resulting independent DC links, soft switching inverters feed medium frequency voltage to transformer windings, that are wound around one common magnetic core, adding their flux to the total flux in the core. On the secondary LV side, one winding and following rectifier is applied. In this topology, the advantages of fast switching semiconductors can be fully exploited, since the high voltage is divided over a series connection of high frequency converters. Galvanic isolation is given by the medium frequency transformer, leading to a compact high voltage power converter. Further, the system features a high grade of modularity and a DC terminal on the low voltage side.

A modular high voltage DC/DC converter is derived from the afore discussed medium frequency transformer by dissolving the common magnetic circuit and converting the HVAC into a HVDC terminal. Therefore, the inverters of frequency converters are removed and the DC links are connected in series. Three layouts for the proposed converter are given in Figure 3.1. The shown layouts are for LV to HV, HV to LV and HV to HV voltage conversion in Subfigure (a), (b) and (c), respectively. In the Figure, the modules are simplified to converters, consisting of full bridge inverter and rectifier and a transformer for voltage conversion and galvanic isolation. The resonance elements and the low voltage DC capacitors are not shown for clarity of the overview. On the LV terminal side, the modules are connected in parallel, each module experiences the full terminal voltage, the terminal current is divided to the modules. On the HV terminal side, a capacitive voltage divider is formed with the DC capacitors $C_{\mathrm{i1}} \ldots C_{\mathrm{iN}}$ and/or $C_{\mathrm{o1}} \ldots C_{\mathrm{oM}}$, of the in- and output side, respectively.

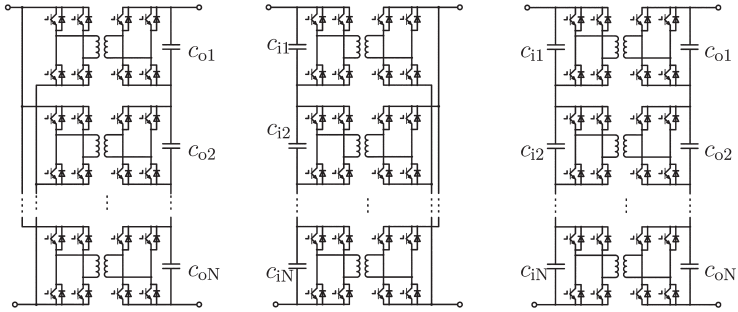


Figure 3.1.: Simplified high voltage DC/DC converter structures, (a) with low voltage input and high voltage output terminal, (b) high voltage in- and low voltage output and (c) high voltage in- and output terminal

The DC capacitor voltage is equal to the voltage V_{Mod} on the single module terminal and is averagely related to the converter terminal voltage by the voltage divider rule

$$V_{\mathrm{Mod}} = \frac{1}{N} V_{\mathrm{dc}}, \tag{3.1}$$

where N is the total number of modules, that are connected in series. The nominal power of one module is the N^{th} of the complete converter. The terminal current runs through all modules in series – buffered by the DC capacitors. This way, the semiconductors in the modules experience only a fraction of the high DC voltage, and hence, semiconductors with less blocking voltage can be utilized. Then, the advantages of low voltage DC/DC converters can be exploited. Such a modular high voltage DC/DC converter has been described by Reinold in the patent [Rei02], with center taped DC terminals and resonance circuits featuring one series capacitor on each side of the transformer.

The most obvious advantage of modular structures is the easy customizability of the converter to various application scenarios by variation of the number of modules in order to match the requirements for the application at hand. The argumentation is comparable to the one for other modular converters, such as modular multilevel converters. This modularity exists only to a certain degree, if one common magnetic core is used, hence it was eliminated in the given design.
Compared to monolithic, non-modular converters, modular converters are inherently more reliable. If single modules break down, the remaining modules are still capable of converting power. Therefore, the broken converters are shortened in the series

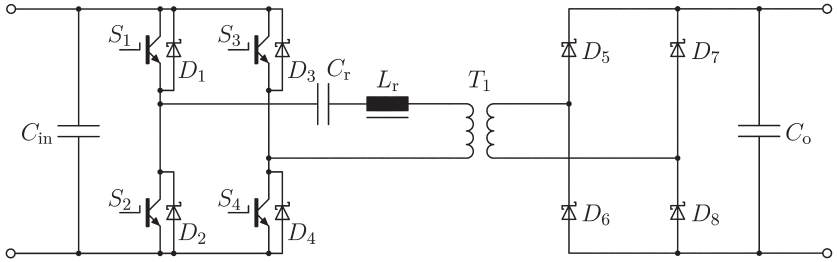


Figure 3.2.: Basic schematics of an LLC resonance converter with full bridge inverter and rectifier and transformer

connection and turned off on the parallel side with the existing semiconductor switches. The overall converters power and HV terminal voltage must then be reduced by the part of the failed module. The converter can be operated at reduced power, until the malfunction is dissolved. Additional shortcut switches over the series capacitors and breakers in the parallel connections solve the dependence from the semiconductors and increase the systems reliability. To further increase the system reliability, additional spare modules can be added to the system. These modules are fully connected but do not participate in the conversion process. In case of a breakdown, one of the spare modules is activated, the converter can operate at full rated power and voltage and the defective parts can be replaced at the next scheduled maintenance.
A side effect of the modularity, compared of monolithic converters, is a new grade of geometrical freedom. The individual modules can be organized to be fitted into available space or in another way that fits the given requirements e.g., good accessibility for maintenance/replacement.
On the systems downside stands a relatively complex system with a high number of potentially expensive semiconductors and a large number of drive signals.

3.2. Conception of a Module for a High Voltage DC/DC Converter

The DC/DC converter, presented in this publication, is intended for use in high voltage applications, where equal modules are combined to one converter, that is capable to convert the multiple of the power and withstand the multiple of terminal voltage of one single module. The modules are required to feature high power density and good energy efficiency. Further, galvanic isolation is required on the module level.

As the current state-of-the-art, resonance converter types exhibit the best energy efficiency and the highest fast switching capability – as long, as they are operated in resonance condition. The incorporation of a transformer for gain adaption and galvanic isolation is possible. Under the resonance converter topologies, with the LLC converter a wide load range can be covered while resonant switching is maintained, the transformer participates in the resonance action and the frequency range, required for voltage control, lies within a reasonable value range. Additionally, this converter type is well known, not too complicated in design and therefore, extensive literature exists. Resonance tank topologies with higher orders would also technically fit the problem at hand, but the increase of system complexity by utilization of such a topology stands out the practical value of its use. Hence an LLC resonance converter with full-bridge inverter and rectifier and a transformer for output voltage adaption and galvanic isolation is chosen.

The LLC converter topology is discussed in Section 2.3, the full-bridge inverter/rectifier layout is given in Figure 3.2, with L_{M} being implicitly given by the transformers primary side windings magnetizing nature. The converter in the Figure features the input terminal on the left side, with a DC blocking capacitor C_{in} for filtering means, followed by the IGBT full bridge inverter $S_1 \ldots S_4$. The resonance circuit C_{r}, L_{r} and the transformer T_1 are in the figures center, on the right side are the full bridge rectifier $S_5 \ldots S_8$ and the DC filter capacitor C_{o}, for filtering the DC output voltage V_{o}. The LLC resonant tank topology, unites high efficiency and power density over a wide range of load and gain variation. The converter modules subcomponents will be discussed in detail in the following sections.

3.2.1. Design Considerations for the Inverter and Rectifier

For the inverters, basically the two bridge layouts shown in Figure 3.3 are relevant: the half bridge and the full bridge layout. A half bridge consists of two bridge arms with switches S_1 and S_2. One DC pole is directly connected to one phase of the AC side (commonly $L2$ to the minus $(-)$ pole, see Figure). The other AC phase $(L1)$ is connected to the plus pole $(+)$ via the bridge arm, consisting switch S_1 and to minus by the one with S_2. If the switches are alternatingly turned on and off – with inverted switching pattern between S_1 and S_2, the voltage between $L1$ and $L2$ oscillates between zero and V_{dc}, the effective voltage of the resulting square wave is $V = {}^{V_{\mathrm{dc}}}/_{2}$. The transferred energy for one full cycle is drawn from the DC side in the first half of each switching cycle when S_1 is conducting. In the second halve cycle, when S_2 conducts, the AC current is reverted and circulates in the resonance tank, while re-magnetizing the transformer core antipolar to its former polarization, the

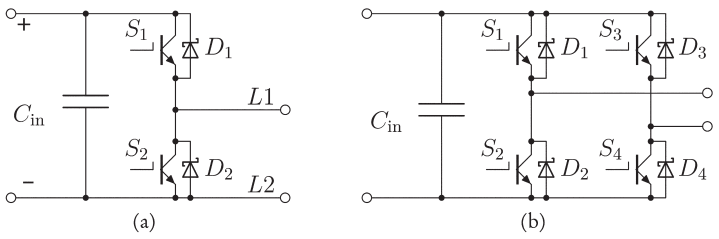


Figure 3.3.: Basic inverter layout in half- (a) and full bridge (b) configuration

energy stored in the resonance tank is transferred to the secondary side. Therefore, the DC current is unsteady with large amplitudes, hence a large input blocking capacitor C_{in} must be utilized to effectively block out EMI. A full bridge (Figure 3.3b) has four bridge arms with semiconductors $S_1 \ldots S_4$. DC plus and minus are alternately conducted to the AC-poles $L1$ and $L2$, the voltage oscillation on the AC side is symmetric to zero (e.g., − potential) and the effective voltage $V = V_{\text{dc}}$ is twice as high as the one of the half bridge output for equal V_{dc}. The load current effective value is half as high, as the one of the half bridge's for the same inverter load. Energy is drawn from the DC side in every half cycle, which, additionally to the lower effective AC current, reduces the DC current amplitude. Therefore, the blocking capacity C_{in} can be reduced to ca. $1/4$ of the blocking capacity for a half bridge, while maintaining the same filtering effect at equal conditions. This is beneficial in high power applications, where the switching frequency is strongly limited by the applied semiconductor switches.

During conduction, in a half bridge, the current is always led through one bridge arm. In a full bridge, the current flows through two arms. Thus, the conducting resistance from the switches $R_{\text{on,full}}$ is twice as high in a full bridge, as the on-resistance $R_{\text{on,half}}$ in a half bridge. Therewith, the conducting losses of the full and half bridge can be set to the relation

$$P_{\text{v,full}} = 2R_{\text{on,half}} \cdot \left(\frac{1}{2} I_{\text{half}}\right)^2 = \frac{1}{2} P_{\text{v,half}}, \tag{3.2}$$

where $P_{\text{v,full}}$ is the conducting loss of the full bridge and $P_{\text{v,half}}$ the one of the half bridge. Thus, it is recognized that the conducting losses in the semiconductors of a full bridge are $1/2$ of the ones in a half bridge configuration, for the rectifier, the derived relation of the full- and half bridge loss holds true as well. For actively switched bridges, in full bridges, the driver must be capable to charge twice as much gate capacitors per switching cycle as for a half bridge. In resonance converter topologies,

the majority of bridge losses are conducting losses, since switching losses are reduced by the strategy of zero current or zero voltage switching. Hence, especially in high power applications, the reduction of the conduction losses by applying full bridge inverter and rectifier is reasonable, even with the larger bridge footprint, that partly consumes the space savings of the DC capacitors. Considering the given discussion, a full bridge configuration is chosen for the inverter and rectifier of the presented converter module.

The current in LLC-type resonant converters describes a waveform, where the semiconductor switches are turned on under zvs condition and turned off, while only the magnetizing current flows through them. This comes close to an ideal waveform for MOSFETs [Hua10]. This is the reason why these switches are widely used in LLC converters. However, studies on LLC converters featuring IGBTs exist in literature, e.g., in [IA06, SML+13]. In high voltage, high power applications, IGBTs present the state-of-the-art semiconductor switches, also due to their conducting loss, that is linear against the current, versus MOSFET losses, that are quadratic against the current. Here, IGBT semiconductor switches are utilized, even if MOSFETs are principally feasible.
The choice of the blocking voltage of the active semiconductor switches is a trade off – the lower the blocking voltage, the more modules are necessary for the same total voltage. With increasing number modules, the space for auxiliary circuits and capacitive voltage divider may become larger and over consume the space savings by increased operating frequency.

3.2.2. Operating Space and Conditions of the Converter Module

The operating area of an LLC resonant converter is defined by the range of gain ΔM_{G}, that is required to achieve a defined range of load ΔP_{Load} and the input inverters switching frequency Δf_{sw}, that is required to cover these required gain and load ranges. In accordance to section 2.3, the concept of LLC converters is to operate in zvs turn-on and reduced current turn-off conditions for best efficiency and reduced EMI. To fulfill these operation principles, the corner points of the converters operating area are laid out in a way that the full operating area is located on the negative slopes of the set of converter gain characteristics and the nominal output voltage can be tuned in under all operating conditions.

An exemplary operating area for a resonance circuit with normalized inductance $L_{\mathrm{n}} = 4.4$ and a quality factor of $Q_{\mathrm{e}} = 3$ for full load is given in Figure 3.4. For maximal converter load – which is equal to the highest load quality factor, the primary DC voltage maximally decreases due to non-zero source impedance, hence, the input

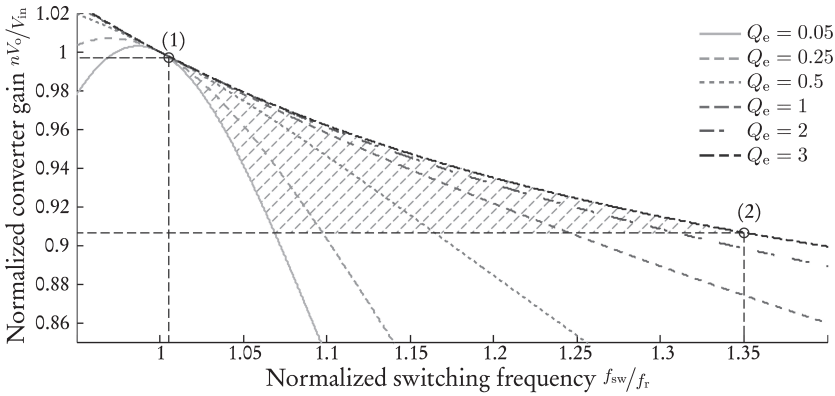


Figure 3.4.: Operating area of an LLC resonance converter with $(f_{\mathrm{sw,min}}, M_{\mathrm{max}})$ being represented by corner point (1) and $(f_{\mathrm{sw,max}}, M_{\mathrm{min}})$ by (2).

to nominal output voltage is highest and the largest converter gain to achieve nominal output voltage is required for maximal load. To meet the converter design requirements of zvs turn-on and reduced current turn-off and maximally exploit the converter gain capability, the corner point (1) is placed on the negative slope of the gain characteristic for $Q_e = 3$ in the vicinity of its maximum. Simplifications in the model, used in the design process and system uncertainties result in inaccuracies of the gain characteristic. For example, a static converter gain function – such as FHA-equations, introduced in section 2.3.2 – neglects the effects from the inverter and semiconductor, e.g., the voltage drops on semiconductor junctions and ohmic loss in the converters and in the AC circuit, the resistance of the conductors and the secondary leakage inductance is neglected. These inaccuracies result in a deviation of the real converters versus the models gain characteristic. With a precise model the deviation can be kept small but cannot be eliminated. Therefore, it is common praxis to add a safety margin between the gain maximum and the upper corner point (1). Corner point (1) is located at the maximal converter gain

$$M_{\mathrm{max}} = n\frac{V_{\mathrm{o,nom}}}{V_{\mathrm{in,min}}}, \tag{3.3}$$

that the converter must be capable to tune in under full load to reach the specified nominal converter output voltage $V_{\mathrm{o,nom}}$ at the lowest assumed converter input voltage $V_{\mathrm{in,min}}$. This operating point represents the minimal converter switching frequency $f_{\mathrm{sw,min}}$ of the designated operating area.
Due to low current at low load or idle state, the source voltage digression and internal

voltage drop in the converter is minimal in the idle state, concomitantly the secondary DC capacitor voltage is maximal for this condition at a given switching frequency. Hence, the minimal converter gain M_{min} is required for minimal load – which is represented by the $Q_{\mathrm{e}} = 0.05$ gain characteristics in the Figure. To cover model uncertainties, the achievable output voltage for idle should be reducible to the minimal converter output voltage $V_{\mathrm{o,min}}$ at nominal input voltage $V_{\mathrm{in,nom}}$, which occurs for an unloaded voltage source, therefore the minimal gain is

$$M_{\mathrm{min}} = n\frac{V_{\mathrm{o,min}}}{V_{\mathrm{in,nom}}}. \tag{3.4}$$

That operating point is located at the highest switching frequency $f_{\mathrm{sw,max}}$ of the operating area and defines corner point (2) in the Figure. The converter switching frequency is technically limited by the fast-switching capability of the inverter and rectifier semiconductors, if $f_{\mathrm{sw,max}}$ is located close to the upper semiconductor switching limit, the converters fast switching capability is used at its best, which allows it to be designed as compact as possible with given semiconductors.
With the foregoing discussions, the converter's operating area is represented by the hatched part in the Figure, it is limited from left by the gain characteristic of the quality factor $Q_{\mathrm{e}} = 3$ representing the maximal converter load, from below by the minimal converter gain M_{min} and from top by the maximal converter gain M_{max} and the minimal load that is represented by the gain characteristic of $Q_{\mathrm{e}} = 0.05$. The intersection of the minimum load curve and M_{min} is located at corner point (2), where the maximal switching frequency occurs.

In the design process, preliminary to the detailed resonance tank and transformer parametrization, the basic framework of the converter operating range is set by the maximal and minimal converter gains in equations (3.3) and (3.4), respectively. This will be followed by the design of the transformer for a designated resonance frequency f_{r} and an adequate normalized inductance L_{n}. The process and its accompanying considerations are presented in the following section.

3.2.3. Design Considerations for the Transformer and the Resonance Components

The transformer of the LLC converter is depicted by T_1 in the converter schematics in Figure 3.2. In resonance converters the transformer can be part of the resonance circuit, besides its function for gain adaption and galvanic isolation. For LLC converters, this is common and adds further aspects to the transformer design process. Regarding the resonance circuit, the transformer contributes to the resonance action by its primary

leakage inductance L_1, that adds to the series resonance inductance and in partial and no load conditions, the transformer magnetizing inductance L_M adds to the internal dynamics as parallel resonance inductance, resulting in the second resonance frequency $f_{\mathrm{r}1}$. Like in any other converter, the static converter gain is adapted by properly setting the transformer winding ratio, e.g., by resolving equation (3.3) to n.

The transformers secondary winding can be center tapped with connection of the center to the negative DC terminal. The full-wave AC current is rectified through the outer taps, that are connected to positive DC via rectifier diodes. The center taped configuration spares two diodes versus the full bridge configuration. Assuming equal system specifications, the center tapped transformer configuration requires to fit many as much secondary windings into the same space as the transformer for the full bridge rectifier, hence the copper cross section is halved, yielding $2R_2$ for the secondary resistance, if the full bridge transformers secondary resistance is R_2. The transformer secondary side for full bridge rectification carries the complete current I_o, hence the total loss in the secondary side yields

$$P_{\mathrm{v,Tfb}} = I_\mathrm{o}^2 R_2 + 2P_{\mathrm{v,D}} \tag{3.5}$$

for this setup, where $P_{\mathrm{v,D}}$ is the conductive power loss within one single diode. In the center tapped transformer setup, each half winding carries the current $I_\mathrm{o}/2$. With symmetrical construction of the current paths for the positive and negative half wave, the converter secondary sides total loss for center tapped design yields

$$P_{\mathrm{v,Tct}} = 2 \cdot \left(\frac{I_\mathrm{o}^2}{4} 2R_2 + P_{\mathrm{v,D}} \right) = I_\mathrm{o}^2 R_2 + 2P_{\mathrm{v,D}}. \tag{3.6}$$

In conclusion, equations (3.5) and (3.6) yield equal relations for the loss within the converters secondary side for the full bridge and the center tapped transformer rectifier configuration. Limiting to the above statement, the full bridge transformer requires few additional windings to compensate the voltage drop of the second diode, which finally puts the center tapped configuration to slight advantage regarding the energy efficiency.
In reverse blocking operation, the rectifier diodes experience the voltage of the full transformer secondary winding from one outer terminal to the second, which is

$$V_\mathrm{dr} = \hat{v}_2 - V_\mathrm{df} \tag{3.7}$$

for the full bridge rectifier, where v_2 is the transformer secondary winding voltage and

$$V_\mathrm{dr} = 2\hat{v}_2 - V_\mathrm{df} \tag{3.8}$$

for the center tapped transformer setup. With $V_{\mathrm{df}} \approxeq 0$, the rectifier diodes on the center tapped transformer experience approx. the double transformer output voltage than in the full bridge rectifier setup.

Concluding the forgoing discussion on full bridge rectifier versus center tapped transformer configuration, for both configurations reasons for implementation can be found and both are widely used in power converter applications. For the modular DC/DC converter, a further aspect of consideration is the installation of spare modules in series connection. These spare modules are fully connected to the converter but are turned off while not in use. Consequently, in the HV configuration, where the module output terminals are series connected, the output current runs through the rectifiers of the turned off spare modules. In the center tapped transformer configuration, the current will be divided at the center tap and from there runs through the transformer secondary half-windings and the rectifier diodes. The transformer windings then cause an inductive voltage drop, due to the quasi $|\sin|$-nature of the unfiltered DC current. At the full bridge, approx. one half of the current runs through each rectifier arm, no current runs through the transformer, the voltage drop on the diodes is twice as high, as in the center tapped transformer configuration, but no inductive voltage drop occurs. Hence, the full bridge rectifier is preferable over the center tapped transformer configuration.

For the transformer design, the dedicated operating frequency and load is essential. For resonance converters, that operate with variable frequency, the operating point with the highest stress to the transformer is of interest. The magnetic flux in the transformer core is inversely proportional to the transformers operating frequency, hence, the highest peak flux is reached at $f_{\mathrm{sw,min}}$ and the transformers turn numbers are evaluated for this frequency to avoid core saturation. For LLC converters, this is the frequency of operating point (1) in Figure 3.4, in the vicinity of the higher resonance frequency f_{r}. The static transformer gain $n = {}^{N_1}/_{N_2}$ can be obtained from equation (3.3) or (3.4).
Commonly, the transformer turn ratio is corrected to compensate the internal inductive voltage drop. For LLC converters it is argued, that the primary leakage inductance participates in the resonant action and hence, no winding correction is required. On the other hand, at least the secondary leakage inductance causes internal voltage drop. Hence, the correction should be executed, to ensure the required gain margin is reached.

A key parameter of LLC converter design is the normalized inductance L_{n} (introduced in section 2.2.2) determining the steepness of the converter frequency-gain characteristics. The gain characteristics for various L_{n} in the frequency range of the resonance frequency are given in Figure 3.5. The graphs are drawn for an equal

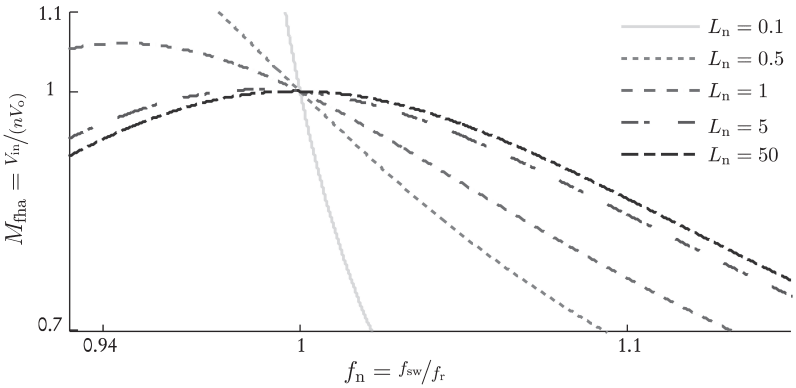


Figure 3.5.: Gain characteristics of different L_{n} under quality factor $Q_{\mathrm{e}} = 3$

primary side equivalent quality factor of $Q_{\mathrm{e}} = 3$, the graphs axes are normalized to f_{r} and nV_{o}, respectively. For small L_{n} values (e.g., < 1), the gain experiences steep deviations around the resonance frequency, converter gains above unity can be achieved and small increases of L_{n} strongly effect the gain curves steepness. With increasing L_{n}, the maximally achievable gain decreases, the curves become flatter and the effect of varying L_{n} generally loses significance. Steep gain curves allow fast control by only slight adjustment of the operating frequency. The closer the converter is operated at the resonance frequency, the smaller the magnetizing current becomes in the turn-off instance of the semiconductor; hence, turn-off losses will be lower. If a digital voltage controller is used to determine the converters operating point, the switching frequency will be quantized due to the time discretization of the controller's digital output. Hence, with increasing steepness of the gain curves, the accuracy of the achievable output frequency will suffer. The realized L_{n} will then be a fitting trade-off between dynamic and accuracy. The value for the resonance inductance L_{r} is then determined from the transformer magnetizing inductance and the desired gain characteristics.

With known L_{r}, the resonance capacitance C_{r} is dimensioned according to the desired resonance frequency. The voltage stress on the resonance capacitor increases with increasing load quality factor Q_{e}. The peak-to-peak amplification of the input voltage on the capacitor $\hat{v}_{\mathrm{Cr}}/V_{\mathrm{in}}$ versus the normalized operating frequency is given in Figure 3.6 for various Q_{e} between 1 and 3, and for $L_{\mathrm{n}} = 4.4$ with a full bridge inverter. The capacitor voltage describes a curve form that is roughly comparable to the curve form of the input to output characteristic, with a maximum around the resonance frequency. Towards low frequency, the gain only slightly decreases,

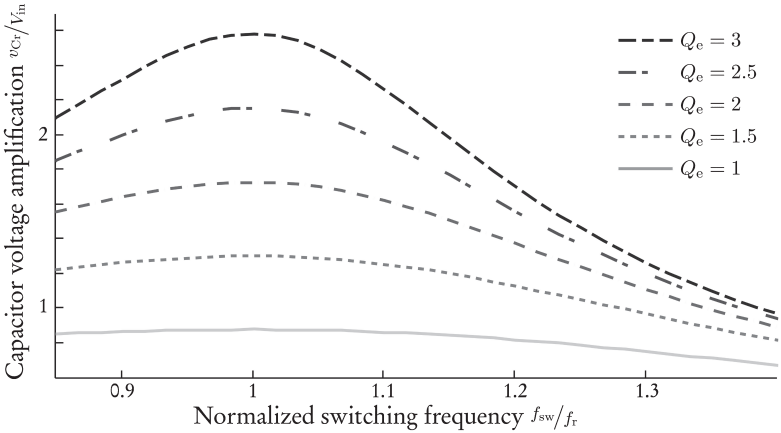


Figure 3.6.: Resonance capacitor voltage amplification versus DC input voltage for quality factors Q_e between 1 and 3 at $L_n = 4.4$

while towards higher frequencies, it converges relatively quickly to zero. On that account, the maximal voltage stress on the resonance capacitor occurs at maximal load, which is the uppermost curve and where the converter is operated closest to resonance. If a half bridge inverter is used, the capacitor voltage amplification is half the full bridge amplification due to the halved AC input voltage of the resonance circuit. Consequently, in the design process, the capacitor voltage must be evaluated under allowance of the normalized inductance and the load quality factor.

3.2.4. Galvanic Isolation and Handling of Different Electrical Potentials

The galvanic input to output isolation of the modular DC/DC converter is implemented on the module level. Therefore, the complete module must be input to output isolated, including the power circuit and all relevant auxiliaries, namely the drive and sensor circuits are isolated, first against the opposite power side (e.g., primary or secondary side) and second, against the control computer. A converter module with its power connections and auxiliary circuits is given in Figure 3.7. The primary energy source is the three-phase electrical AC grid in the top left corner of the Figure, it supplies energy for the DC/DC converter's purpose (e.g., power delivery to a DC load) and possibly to power the converters control computer and auxiliaries. After

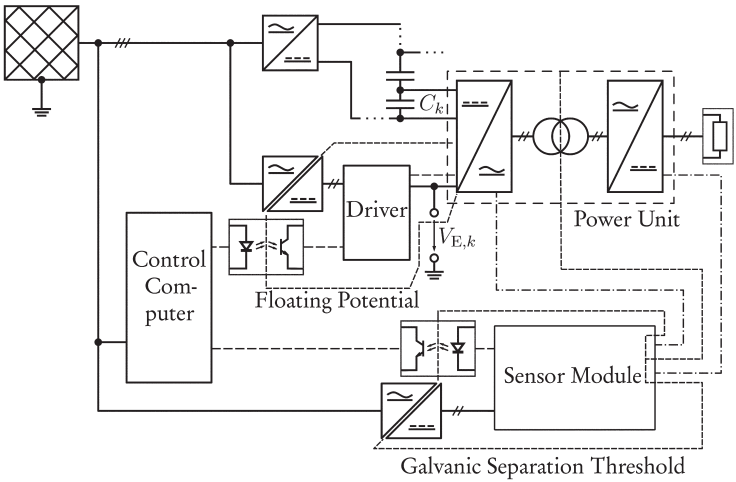


Figure 3.7.: Galvanic separation concept and potential visualization for series connected converter modules in a modular DC/DC converter, depicted for the k^{th} converter module

rectification of the AC voltage, the converter modules are connected, in the example, they are connected in series to demonstrate the occurrence of different potentials in the auxiliary circuits. The series connection is illustrated by a capacitive voltage divider with doted conductors, the input terminal of the power unit of one converter module is connected to capacitor C_k, representing the k^{th} converter module. In the following, the measures to achieve full galvanic isolation are described with reference to the figure.

The LLC converters power circuit is inherently input to output isolated by the transformer with galvanic isolation for the occurring electrical potential in the converter circuit. The electric potential, that effects the isolation of the transformer is the clamp voltage of one single module, hence the transformer isolation must only withstand the module clamp voltage [Rei02]. With less isolation, windings can be tighter and primary and secondary windings can be closer to each other which results in better use of available space and compacter transformers with better coupling, less leakage inductance but more parasitic capacitance.

In most cases, auxiliary circuits from the power converters primary and secondary side are connected to the control computer, e.g., inverter drives on the primary and sensors on both sides, in the Figure, the sensors are summarized in the Sensor Module

in the Figures lower right. The dashed lines depict the connection to the primary and the secondary converter side, which are isolated from each other. The signals are routed to one potential within the Sensor Module. In series connected converter modules according to Subfigures 3.1b or 3.1c, additionally the electrical base potential on the primary side $(-)$ pole of the module is $V_{\mathrm{E},k} = V_{\mathrm{in}}(N-k)$ for the k^{th} module, according to Figure 3.1. Due to the direct connection of the driver circuit, it floats on the same electrical potential $V_{\mathrm{E},k}$ as the module's power circuit, depicted by the base connection in Figure 3.7. Although contactless voltage and current sensors exist, they are seated at the upper end of the cost scale and hence are only used in case of necessity. Consequently, sensors are connected to the power circuits and occurring electric potential must be investigated. To connect auxiliaries with non-zero electric potential to the converters central control computer, they must be galvanically decoupled against each other and against the control computer to maintain the input to output isolation and avoid shortening of the series connected modules. Additionally, to the given reasons of galvanic decoupling, the control computer is protected from residual currents and over voltage in case of module faults by including galvanic isolation between all module connections and the control computer. The voltage, that must be galvanically decoupled in the drive circuits is the largest electric potential between driver modules, which is the full converter voltage V_{in}.
The control signals for the driver modules are of binary nature, hence, magnetic transducers or optical solutions can be implemented for galvanic decoupling. Magnetic transducers cannot transmit constant high signals: once, the magnetic core saturates or the input signals current limit is reached, the output voltage drops to zero, which is not practicable for static signals, as enable or other status signals, that remain constant during converter operation. An optical transmitter is depicted in the figure. In the signal wiring from the control computer to the driver module, optical transmitters have no saturation and draw constant current in high state. Constant signals can be securely transmitted. For the sensors different solutions exist. The commercial marked offers a broad spectrum of voltage and current sensors with integrated galvanic isolation that can be utilized at least up to a certain voltage level or for module level isolation. For additional isolation e.g., for higher voltage levels of the complete converter, a suitable solution could be the digitalization of the analog sensor signals and transmission to the control computer via optical line by use of a serial bus protocol.

To maintain the desired electric potentials, additional galvanic separation must be implemented in the power supply circuits of the auxiliaries. From the above discussion on electrical potentials for the driver circuits and the visualization in Figure 3.7, it becomes clear, that each driver requires an individual power supply with according isolation level, that must withstand the full converter voltage. If the internal isolation of the sensors is sufficient, one single power supply for all sensors may be used, otherwise, the sensors need an isolated supply per converter module and the supply is

to be input-output isolated. For cases where primary and secondary side sensors are treated separately, the power supply is also to be treated separately.

3.3. Application Scenario I: HV DC/DC Converters for Grid Connection of Offshore Wind Farms

In the following, the current state-of-the-art of wind energy systems in industry, focused on offshore wind farming, is summarized, mainly based on information in Chapter 7.2 of the 2013 textbook [KSW13] by Kaltschmitt et al. It provides comprehensive information on wind energy systems. In state-of-the-art electrical energy generation from wind, the wind energy is captured by a wind turbine, that drives an AC generator – usually via a gearbox – at variable wind speed driven speed. The connection to the electrical grid can be of direct or indirect nature. For the direct grid connection, the generator output must be fitting in frequency, hence synchronous generators must run at a certain constant speed or asynchronous generators must be used to allow variable drive shaft speed, at least to a certain degree. Constant speed limits the tracking capabilities of the maximum power point (known as Maximum Power Point Tracking (MPPT) technique). Reactivity towards wind speed unsteadiness of the wind turbine is the reason why these systems are not used any longer. With indirect grid connection, the generator speed can be variable to run at optimal speed, the resulting electrical energy is then frequency converted to grid voltage and frequency (e.g., 50 Hz, in Europe). The conversion feasible via direct frequency converters or AC/DC, DC/AC conversion with DC voltage or current link state-of-the-art large scale wind turbines, commonly features AC/DC, DC/AC conversion with DC voltage link. Electro-mechanical components and the power converters are hosted in the turbine's nacelle. Currently, large scale wind turbines are seated in the multi megawatt (MW) range. Total wind farms are currently going up to the three-digit multi-MW range. On offshore wind farms, the 50 Hz AC voltage output of all turbines is transferred to a collecting station. From there, it is either directly transmitted to shore via sea cable, transmitted via HVAC, or converted to HVDC for transmission. Today AC transmission is the standard [HBM+13]. Ashore, the offshore wind power is either AC/DC converted or transformed to grid voltage and fed into the electrical grid. [KSW13, Ch. 7.2]

Cable systems, especially in sea water environment, feature a large per meter capacitance, that causes large reactive compensation currents, when operated in AC. The reactive current increases with increasing voltage and transmission distance, causing losses in the transmission cable if they are not compensated by compensation

equipment. However, in DC operation, where no capacitive current flows, due to the absence of skin effect and dielectric loss, less conductor material for equal current and less isolation material for the same voltage is required. [HBM+13], [OO11, Ch. 19.4] To gain these advantages, costly and loss generating converter stations on both sides of the HVDC line are required. From an economical position, HVDC becomes interesting with large transmission distances, where additional cost for the converter stations is super-compensated by the absence of reactive transmission losses and less costy cables. For sea cables, the distance for equality of cost for HVAC and HVDC transmission is given for $80\,\mathrm{km}$ in [KSW13, Ch. 7.2], in [OO11, Ch. 19.5] this distance is given as 20 – $50\,\mathrm{km}$, above HVDC is preferable.
The rest of this section discusses options to enhance wind energy farming systems by application of modular DC/DC converters. The focus is set on large scale offshore plants with HVDC transmission, according to [KSW13, Ch. 7.2], future offshore wind farms will likely scale up and be located further away from shore, which presents a classical DC application scenario. [OO11]

In the future, the transmission of wind energy from offshore wind farms will likely be executed by HVDC sea cables, especially for large wind farms that are far away from shore. This means, that the wind farms main electrical interface for energy transmission applies HVDC, while current state-of-the-art wind farms are internally wired with an AC grid with relatively low voltage – with all the above discussed drawbacks of thick cables, losses due to capacitance and high current, etc. Further, additional platforms for high voltage transformation and rectification units are required at the offshore site, further driving effort and cost of the wind farm. [HBM+13, MP15] Alternative, all DC wind farm architectures were proposed in academia, where wind turbines output DC voltage. A number of turbines is then series connected to form HVDC, that is directly transmitted to shore – without need of grit frequency transformers and rectifiers with according platforms on site, e.g., by [RJJ10, HBM+13] and [MP15]. The fundamental layout of such an offshore wind farm is depicted in Figure 3.8a. A number of equal wind turbines generate DC output at their outer terminals A_k and B_k. The DC outputs are connected in series to achieve the dedicated voltage for the HVDC sea cable. On the shore side (right part of the figure), another DC/DC conversion is undertaken before the electrical energy is inverted and fed to the electrical grid. This general structure is equal in most papers, but varies in details as the DC voltage generation in the wind turbine. In [HBM+13] and [MP15] for example, a conversion stage with Medium Frequency (MF) transformer is proposed, the MF is generated either by AC/AC conversion with voltage lank, a matrix converter in [HBM+13] or AC/AC conversion with current link in [MP15]. If a multiple of the series connected turbines exist, either turbines, or strings of series connected entities are paralleled. For the grid connection, [MP15] proposes a series connection of a number of input series, output parallel connected

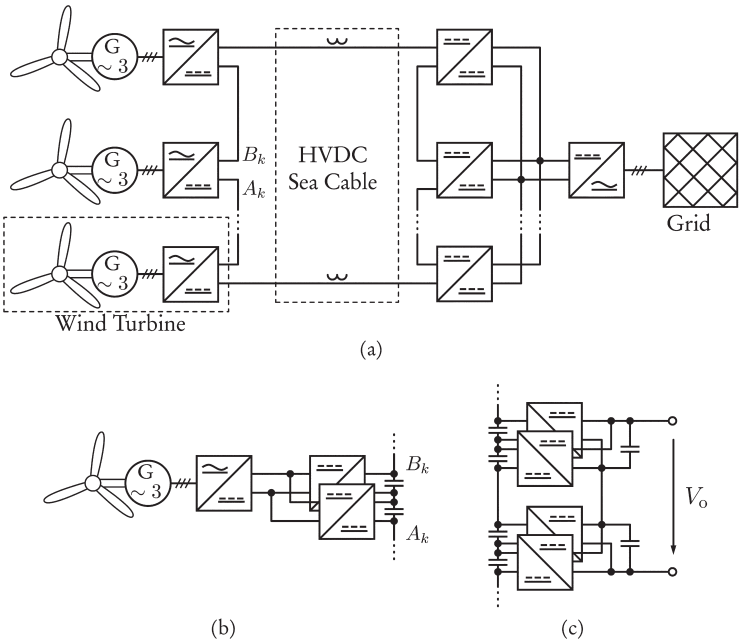


Figure 3.8.: (a): All DC offshore wind farm with series connected wind turbines, generating high DC voltage, HVDC transmission to shore and concentrated, modular high voltage DC/DC converter and inverter for grid connection. (b): Wind turbine with modular, high voltage DC/DC converter for all DC wind farm application

modules for a number of grid connections. According to [HBM+13], all-DC wind farms profit from large entity power in form of increased reliability and reduced cost, for 10 MW turbines, cost for DC systems is reduced by 8 % versus the AC version, reliability is still worse than for AC, but the gap decreases. The total wind farm efficiency for all-DC with DC voltage link in the nacelle is given with 10 % below and with matrix converter with 10 % above AC-level respectively.

For such an offshore wind farm architecture, the modular high voltage DC/DC converter could be utilized in a distributed manner on the wind farm side and concentrated on the shore side. The utilization of the modular DC/DC converter from in this publication in the nacelle of an offshore wind turbine is given in Figure 3.8b: The generator's electrical AC output is rectified, to this DC voltage link, a DC/DC

converter is connected – in the figure it is a two stage, parallel input series output converter. The turbines outer terminals are marked by A_k and B_k again. The converters internal setup can vary in number of modules from one to an undetermined number, and in terminal configuration from parallel input - parallel output to series input - series output or a combination of parallel/series terminals, depending on the power and voltage ratings of the turbine. For low power ratings, for example one single module is sufficient, while with increasing generator power, more modules become reasonable. Then, a higher output voltage can be obtained, by the output series connection. Less series connected wind turbines are required to reach a certain transmission voltage, depending on the generator's voltage rating, the converter input is parallel or series connected. The converter output presents the wind turbine terminal to the wind farm, together with the neighboring turbines, one string of a modular high voltage DC/DC converter is formed. The DC/DC converters galvanic input to output separation implements the isolation of the turbine's electrical equipment from the high transmission voltage. These components must not be isolated for HVDC level [MP15].
If more wind turbines are located on the wind farm than are connected to one string – a string is the series connection of a number of wind turbines to form transmission level voltage, either multiple strings can be connected to the transmission line, or some wind turbines are paralleled at A_k and B_k before being integrated into the string. On the shore side, a modular DC/DC converter with equal modules is utilized to convert the electrical wind energy from HVDC transmission level to grid voltage level and for galvanic isolation of the grid from the high transmission voltage. The series input, parallel output in Figure 3.8a depicts a simplified setup, large scale offshore wind farms are usually connected to the high or extra-high voltage AC grid (in Europe up to 380 kV), which is above the scope of the voltage level of one module, hence this will more likely be a series/parallel combination of the output terminals, as given in Figure 3.8c, where V_o is the inverter input voltage. Recently, HVDC power distribution is discussed for the European continent under the term *(European) super grid*. The basic idea is to spread a coarsely meshed HVDC grid across Europe for high power shifting across the continent. This is primarily necessary due to increasing renewable energy sources with unsteady power generation such as solar and wind energy. Comparable to the statements in [Rei02], an incoming sea cable can be interconnected to a super grid by a modular high voltage DC/DC converter.

Advantages of all DC offshore wind farms are vastly described e.g., in [HBM+13, MP15] and in the preceding paragraph, still, the improvements gained are treated in by certain drawbacks. In [HBM+13], the loss of MPPT for individual wind turbines, along with reduced all-over efficiency of the wind farm due to the sharing of voltage and current in the series connected entities is recorded. Another issue, closely related to the series connection of the converter modules, is the event of breakdown of

one wind turbine. In the wind farm architecture, implementation of the method of providing spare modules for redundancy according to section 3.1 is difficult, since the modules are not supplied by one common energy source. Spare modules would be needed for every source, driving cost into the extreme. Further, all other components in the energy conversion chain need to be protected against failure. The described issue is discussed in [HBM+13] under reliability, it is stated, that increasing wind turbine power increases DC wind farm reliability, which accords to the here given discussion.

The wind farm efficiency in conventional AC versus all DC setup is evaluated in [HBM+13] by simulation of setups with DC voltage link and matrix converter for both $2\,\mathrm{kV}$ and $10\,\mathrm{kV}$. Results are distinguished by turbine loss and rest of the wind farm. For the $10\,\mathrm{kV}$ setup, the loss for the rest of the wind farm is smaller for DC, the converter loss is ordered AC matrix, DC matrix, AC bridge, DC bridge converter from low to high loss, respectively. The lowest loss for AC matrix converter is $59\,\%$ of the worst performing DC bridge converter. However, the DC/DC bridge converter in the reference is a hard switching PWM converter operating at the tenfold of the transformer frequency of $5\,\mathrm{kHz}$, switching is executed under full voltage and current. To compare resonant converters like the ones proposed here for utilization in modular converters which are not evaluated in the reference, the reduced switching frequency and the reduced rated voltage and current in the switching instance needs to be analyzed. Starting with the switching frequency, and assuming that the MF transformer operating frequency will be kept at $5\,\mathrm{kHz}$, the resonant converter's switches are operated in the frequency of the fundamental current wave, which is approx. the transformer frequency – inaccuracies due to variable frequency operation is neglected for sake of simplicity. According to the graphs in [HBM+13], the efficiency of a bridge converter improves from $85\,\%$ to approx. $98\,\%$ by reducing the switching frequency from $50\,\mathrm{kHz}$ to $5\,\mathrm{kHz}$, conducting loss makes approx. $1\,\%$ of the input power, according to the reference. This leaves $1\,\%$ for the hard switching loss, which is divided to turn-on and -off loss. In the proposed LLC converter, switching loss is reduced by zvs turn-on and reduced current turn-off. In conclusion, the matrix converters efficiency of approx. $94\,\%$ in [HBM+13] lies below the resonant converter efficiency by a factor of approx. three, according to the computations from [HBM+13] and here. The total efficiency of a DC offshore wind farm can be increased above the all-AC level by use of distributed modular DC/DC converters in resonant operation.

3.4. Application Scenario II: HV DC / DC Converters for Tethered Mobile Machine Power Supply

A promising field of application for high voltage DC/DC converters are tethered mobile machines, as they exist e.g., for large bucket wheel excavators [ABB11] and smaller excavators [YFM09] for open pit mining electric load haul dumper for underground mining [JHB14, PSFL14], also cranes in container terminals are supplied with electric energy by tethering cables [Fis99, Joh10]. State-of-the-art tethered mobile machines are supplied and operated with three-phase AC voltage from the grid, e.g., in underground mining environment, the pines electrical power supply is separated from the grid by a transformer. The basic schematics of the electric main components for the power supply of an electrical LHD are exemplarily depicted in the introduction in Figure 1.1. The electrical energy is transmitted from a connecting point near the operating area of the machine via a flexible transmission line. Usually, the transmission voltage is low and hence, the line current is high, requiring large conductor cross sections and heavy cables. On the mobile machine, a motor driven cable reel is mounted. While the machine moves on the ground, the cable tension is held tight by the motor and the reel. If the machine moves away from the connecting point, cable is paid out, dispensable cable is reeled up [YFM09, PSFL14]. To transmit the electrical energy from the cable onto the machine, while maintaining the reels rotability, a set of slip rings is utilized [Con12].

Especially on large machines providing enough space and load capacity like container cranes [Fis99, Joh10] and large bucked wheel excavators [ABB11], a grid-frequency transformer is installed to step the voltage from a high supply voltage down to lower voltage of the machine's electrical infrastructure. In contrast, small machines, like electric loaders for underground operation and even large excavators, are not equipped with a transformer [YFM09, Atl13], and thus, the electric energy is transmitted at machine voltage level. The electrical architecture of such machines is rather simple, consisting of contactors, possibly star/delta starter circuit and induction motors for traction and hydraulic pressure.

In all business cases, independence from rising oil prices, less energy, maintenance and total operating cost are named as driving factors for electrification [YFM09, Joh10]. In [YFM09] the savings of maintenance costs are estimated up to 30 % and in [UIM+13], total operation costs are assumed to be one-half of conventionally powered excavators. Another benefit of the electrification are improved working conditions due to low noise, the absence of exhaust emissions and less waste heat [YFM09, PSFL14], emissions and heat are particularly interesting in underground mining environments, where these may require the installation of costly ventilation systems [PSFL14]. While machines with diesel engines are quick to be refueled, tethered machines don't require

Table 3.1.: Current reduction factors for coiled cables according to standard DIN VDE 0298-4:2013-06 [DIN13]

Coil layers	0	1	2	3	4	5
Current reduction factor	1	0.8	0.61	0.49	0.42	0.38

any refueling at all [PSFL14]. By electrification, increasing the machine's overall power is simpler than with conventional engines. For many processes, the high torque at low motor speed and high motor dynamics are advantageous [PSFL14].
The majority of todays tethered machines are mining machines, ether in underground or open pit mining, for example underground LHDs, repeatedly move on a path to load the overburden onto trucks. This moving pattern and the existence of electricity in mines makes LHDs an interesting application for tethering, no battery recharging or installation of overhead leads for trolley powering is required [PSFL14].

Disadvantages stated in literature are the need for the electrical infrastructure, if not already in existence and less flexibility due to limitations by the cable [UIM+13, PSFL14]. For underground mining machines, cables up to 400 m [PSFL14] and for container cranes, up to 2000 m are available [Con12]. The constant tension and the permanent reeling are stressing to the cable. In harsh environments, the cables experience additional strong attrition [JHB14] resulting in a high risk of cable damage and fast wear. In accordance to [JHB14] cable issues are the main reasons for breakdowns of electric LHDs, resulting in material and down time cost. Due to missing cable management systems, that avoid running over the own, or others' cable or entanglement of cables, this can be avoided by reducing the number of simultaneously operating machines in one area [PSFL14]. Also, maneuverability between sites is limited for tethered machines and requires more planning efforts [JHB14, PSFL14].

In most applications, the required energy is transmitted at the relatively low operation voltage of the machine's electric drives, hence cables with large cross sections are needed to carry the large currents. Additionally, on the coiled-up cables on the reel, the thermal energy, generated from the ohmic loss of the conductor cannot freely dissipate, and therefore must be kept under strong limits to avoid damage to the cable insulation. Table 3.1 gives current reduction ratios for given coiling layers according to the German Standard DIN VDE 0298-4:2013-06 [DIN13]. This reduction of the current carrying capacity has to be compensated by even larger cross sections of the conductors and hence leads to even heavier cables and large reels even for a few hundred meters of cable and the major reason for the above given short operating ranges of currently existing tethered mobile machines.

3.4.1. Electrical Architecture for a HVDC Tethering System for Mobile Machinery

The afore discussed strongly restricted operation range due to voluminous and heavy cables is considered the main technical reason why trailing cable systems do not extend to more applications and industries. Besides, these limitations might also lead to reluctance against the technology at hand by decision makers in the industry, who then may decide to invest in machines, driven by fossil fuels. In applications, where tethered machines are currently present, extended acting ranges can contribute to ease the handling of these machines – e.g., less re-plugging of the supply cables and exploitation of larger mines. Hence, it is desirable to increase the operating range by installing longer and thinner cables on the machine. Thus, the operation voltage of the cable must be increased to reduce the transmission current, so that cables with smaller cross section can be used while the thermal impact on the conductor remains comparable. Therefore, increasing the operating voltage also increases the isolation thickness, which will partly consume the gained volume reduction. For a thinner cable, less space is needed on the reel, allowing more cable to be stored in the same space. Two issues still remain. Firstly, the high transmission voltage needs to be transformed to machine's operation level – if $50\,/\,60\,\mathrm{Hz}$ AC transmission is used, either a large and heavy transformer or a medium frequency transformer system, comparable to the ones, described e.g., in [SR07], needs to be installed on the mobile machine. $50\,\mathrm{Hz}$ transformers are voluminous and quickly reach a weight of a few hundreds of kg. Secondly, with increasing voltage and cable length capacitive losses are rising, counteracting the goal of reduced losses. Due to capacitive losses, cable length and voltage cannot be increased over a certain extend in AC systems. In the conclusion, HVAC transmission will possibly not lead to the significant volume and mass reductions, that are required to extend the ratio of action of mobile tethered machines.
To establish a HVDC energy transmission onto the machine, high voltage DC/DC converters need to be utilized to extend the capabilities of these machines.

An alternative could be a DC trailing cable system, as it is sketched out in Figure 3.9a. From the AC grid power connection, the electrical energy is rectified and converted to high DC voltage by a galvanically isolated modular DC/DC converter, as it is proposed in this work. Therefore, a conversion station, comprising the grid connection, the required safety gear and the DC/DC converter, needs to be installed at site. The transmission voltage can be set to a sufficiently high voltage according to the required cable length, machine power and available storage space – e.g., in the range of 1 – $30\,\mathrm{kV}$. On the mobile machine, a DC/DC converter with high voltage input and machine DC link level voltage output terminal is installed. The

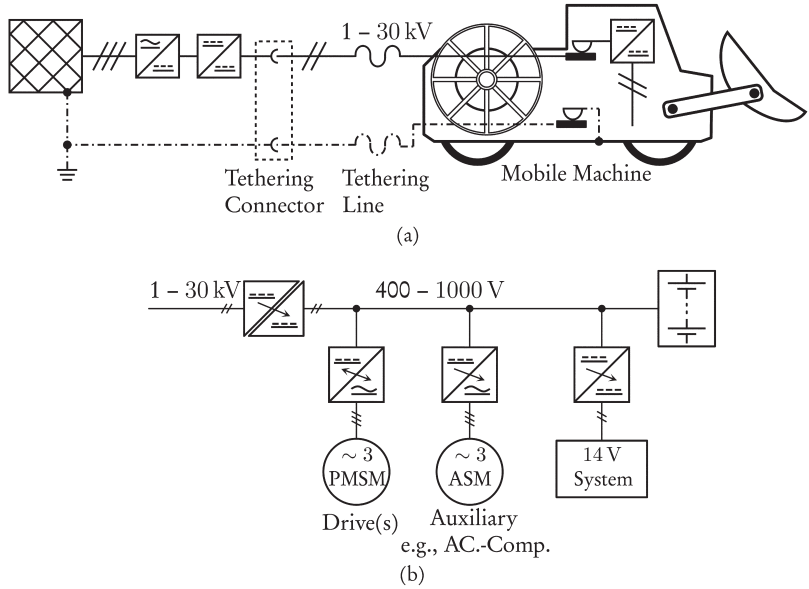


Figure 3.9.: (a): Proposed high voltage DC transmission system for a tethered mobile machine. (b): Exemplary electrical equipment of an electrical mobile machine with optional supporting traction battery.

output terminals of this converter's modules are connected in parallel, feeding the low voltage DC link with high current. The DC link with link voltage between 400 V and 1000 V on the mobile machine is the core of a flexible electrical architecture, that is comparable to the one of electric and hybrid electric road vehicles, an exemplary setup is given in Figure 3.9b. Additional to electric drives, auxiliaries as hydraulic pumps and AC-Compressors can be connected to the link, optionally; a small traction battery can be installed.

The concept of the DC/DC converter in this work features an isolation barrier, such that the secondary circuit is galvanically isolated from the primary one. Such a converter is installed at both ends of the high voltage transmission cable, the trailing cable system forms an IT-net, which is terminated by the converters on the machine and at the stationary connecting point. The insulation resistance of IT-nets versus ground potential can be monitored by isolation monitoring systems, which is mandatory in systems like high-voltage trailing cables for additional safety. In case of a first

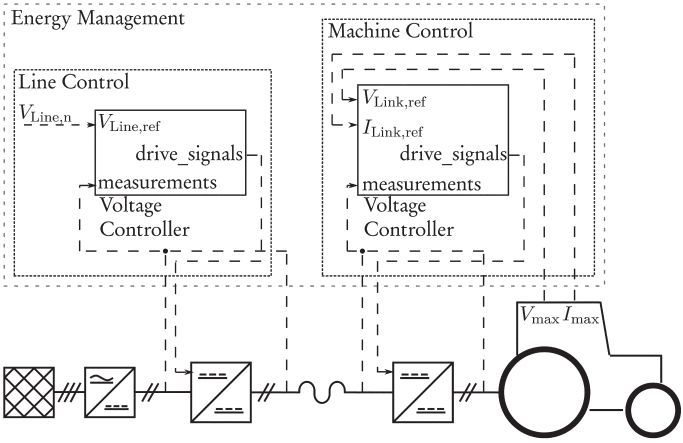


Figure 3.10.: Energy management principle with voltage control at the connection point and load control on the mobile machine

ground fault, only capacitive transient and no continuous current flows against earth and this first fault is detected by the isolation monitoring system. The characteristics of the transient currents depend on the parasitic ground capacities of the system, these must be measured in the real system. [Dip06] The galvanic decoupling of the machine and its electrical equipment from the transmission cable reduces the effective ground capacitance. The usual way to handle a first fault in industrial applications is to indicate it acoustically and / or visually. The high-voltage system can be shut down to further increase the safety in the application at hand.

This HVDC system architecture, optimally fits the transmission voltage to the system power rating. By operating the transmission cable with DC voltage, no reactive power is transmitted, which increases the transmission efficiency of the system and longer transmission distances are possible. Compared to AC voltage converters – especially low frequency transformers, DC/DC converters can be realized with high power density, so that the required extra space and additional load applied to the mobile machine remains reasonable. At the same time, the cable reel mass and volume are decreased due to lower transmission current and hence smaller cross sections. Currently, thinner cables with less copper could also be less expensive, since copper is a driving factor for the cable price at the current marked situation. By choosing a fitting voltage and cross section, the electric power can be transmitted over a reasonably longer distance than with state-of-the-art systems. This overcomes one of the major drawbacks of machines supplied by trailing cables. On the machine itself, the newly

introduced DC link increases the flexibility for the machine architecture. The complete system can be designed e.g., to be optimally energy efficient by optimizing the single drives to their load profiles.
However, the proposed architecture presents a more complex system with possibly more expensive components. Thinner cables are lighter and require less space on the mobile machine but might be less robust against attrition due to a smaller surface and without additional enforcement (e.g., aramid fibers) might have less tensile strength. The limitless increase of the voltage is not reasonable, since the cable isolation has to be thicker for a higher voltage and hence, at a given point, size reduction will come to a limit. With the architecture at hand, the problem of moving machinery between working sites could not be solved. Shutting down the HV system requires a detailed analysis, particularly in emergency cases.

3.4.2. Power Management for a HVDC Tethering System for Mobile Machinery

For the DC tethering system introduced in this Section (3.4), an energy management concept is developed to control the energy flow and ensure the satisfaction of the system's desired operating characteristics. To keep the system complexity low, no communication between the connection point and the mobile machine should be necessary – except for shut down signals in an emergency cases.

The top-level structure of the energy management is outlined in Figure 3.10. In the lower part, the physical system of the DC trailing cable is depicted. The upper part of the figure displays the energy management block diagram. Signals are represented by dashed, arrow-headed lines. The energy management comprises the *Line Control* for voltage control and the *Machine Control* for load control.
The *Line Control* on the upper left side regulates the tethering line voltage to a constant reference value. The controller setpoint is the constant line voltage reference $V_{\mathrm{Line,ref}}$, which is set to the tethering line nominal voltage $V_{\mathrm{Line,n}}$. Line voltage fluctuation, induced by load changes of the mobile machine are leveled out by the voltage controller, guaranteeing stability over the complete load range.
The *Machine Controller* on the Figures upper right side regulates the energy flow from the tethering line to the machine's DC voltage link. For this, the setpoints for the output voltage $V_{\mathrm{Link,ref}}$ and current $I_{\mathrm{Link,ref}}$ of the mobile machines converter are set by the machines internal energy management to V_{max} and I_{max}, respectively, allowing a high flexibility. For example, if a buffer battery is directly connected to the DC link, it might be necessary to limit voltage and current by means of the machine controller to avoid overcharging the battery. For the controllers of the converters

on both sides of the tethering line, measurement inputs are in- and output voltages and/or currents. The control outputs are the drive signals for the semiconductor switches of the converters. By controlling the cable voltage with the converter at the connection point and controlling the energy flow with the converter on the mobile machine, a structure is established, where in normal operation no communication is required.

4. Voltage Control of LLC Converters

The output voltage of uncontrolled DC/DC converters responds to load and input voltage changes due to the internal converter characteristics in the way, as described in Section 2.3. To decouple the output voltage from theses variances, a voltage controller, that computes a drive signal – or the control value u – from the control error e between actual output voltage V_o and according reference signal $V_\mathrm{o,ref}$ is utilized. In resonant converters like LLC converters, the appropriate drive signal is the input inverter's variable operating frequency f_sw. In the minimum, the operating frequency range is limited to the load-dependent minimal value, where the resonance tank is exited at the negative slope of its characteristic voltage gain curves. To the maximum, the operating frequency is limited by the semiconductor switches fast-switching capability. By variation of the inverter frequency, the energy flow through the resonance circuit is controlled, and thereby, the converter voltage gain is adjusted load dependently. Further, the dynamics induced by the output capacitance C_o are of interest, especially in start-up conditions, where the transformer output voltage can rise within a few switching cycles to the nominal output voltage, while a large capacitor charging current flows. In this state, the output capacitor is initially discharged and adds a low impedance to the input to output current path. The given combination of quick voltage rise and low impedance output causes an inrushing current, which can easily reach a multiple of the nominal output current and may destroy the converter's semiconductors. The traditional method to limit the inrushing capacitor current is the utilization of dissipative precharge circuits, where the charge current initially runs through a series resistor, that is shortened, when the voltage across it drops beneath a predefined limit. Alternatively, a converter control strategy can include startup and shutdown routines to effectively limit the inrushing capacitor current – so called soft start routines. For the control design analyzation of the DC/DC converter follows and control strategies are discussed on module level, before the control is extended to a control concept for modular DC/DC converters.

4.1. Mathematical Model of a Modular DC / DC Converter

In Section 2.3.2, a converter model based on FHA is presented from literature. This model characterizes the load depending steady state gain behavior over variable excitation frequency input. To achieve the necessary circuit equations for the model, the converter equivalent circuit is simplified and transferred to an all-AC circuit. In this transfer, the output's DC filtering capacitor is removed from the model, without effect to the model's steady state behavior, which is the only state of interest for the FHA analysis. During load and voltage transitions, the output DC capacitor is charged or discharged, due to load decrease / voltage increase or load increase / voltage decrease, respectively. Hence, during these states, the converter secondary current i_2 differs from the output current i_o, which adds additional dynamics to the system in transient conditions (for details, refer to Figure 4.1). The charge currents and resulting output voltage overshoot and voltage drops are not represented by FHA, therefore, a dynamic model is necessary.
For the mathematical converter model, a detailed electrical equivalent network of the converter is developed. In a first step, the FHA model is enhanced by more detailed converter characteristics, second, the output DC circuit with filtering capacitor and load equivalent resistor is modeled. Based on the circuit models, a set of mesh and junction equations is derived and a state space model expression is formulated.

4.1.1. Electrical Equivalent Circuit for the Converter

Figure 4.1 displays an all-AC electrical equivalent network and one, containing a model of the output DC circuit. In both models, the input is the AC voltage source with variable frequency voltage v_1 from the converters primary side inverter. Its rectangular waveform has the frequency f_sw, its amplitude is quasi constant. The inverter, consisting of four actively driven switches, can be seen as a nearly ideal voltage source. Influences, such as switch voltage drop and dynamics, are neglected in the models. The resonance circuit and the transformers primary winding form the network's primary side. It consists of the resistance of the transformer's primary winding R_1, the resonance capacitor C_r and the total primary side inductance $L_\mathrm{1tot} = L_\mathrm{r} + L_1$, which is the sum of the resonance inductance and the transformer primary leakage inductance in the first arm. A standard electrical model for the transformer with the core lose equivalent resistance R_Fe and the magnetizing inductance L_M is branched from a junction in the vertical and the secondary resistance n^2R_2 and leakage inductance n^2L_2 branches in the horizontal for the converter's secondary AC side. Note:

all secondary side quantities are transformed to the primary side. The transformer primary side carries the current i_1, the core lose causes the current i_{Fe}, i_{M} is the magnetizing current and the secondary AC transformer current is i_2/n. The secondary side is transformed to the primary by the transformer winding ratio $n = n_1/n_2$.
At the all-AC model in part (a) of the Figure, the load is represented by the load equivalent resistor $n^2 R_{\mathrm{L}}$. It is directly applied to the transformer secondary arm, the load voltage is nV_{o}, effected by the secondary AC current.
In literature, the capacitor's dynamics are commonly neglected and the linear model from above, is presented without rectifier. To include the output capacitor's dynamics to the model, the full bridge diode rectifier must be modeled. Diodes are nonlinear components, that can be linearized, if they are only operated in conduction or in blocking mode respectively and in a reasonably small range around a working point. In a rectifier, the diode pairs D_1, D_4 and D_2, D_3 rectify the AC current by alternately conducting the AC current to the DC side and blocking it. Hence, the diodes nonlinearity comes fully into effect and the rectifier cannot be linearized.
To mathematically describe the rectifiers behavior during conduction of the AC current's positive and negative half wave, the signum function of the secondary current can be utilized, i.e., $\mathrm{sgn}(i_2)$, which is added to the advanced converter equivalent circuit with DC output sub-circuit in the Figures part (b).
On the output DC side, the output capacitance C_{o}/n^2 for filtering and the output clamps are connected. The output current I_{o}/n flows through the clamps and is proportional to the variable converter load equivalence resistor $n^2 R_{\mathrm{L}}$.

4.1.2. Branch and Junction Equations and State-Space Model Formulation and Classification

Kirchhoff's circuit laws are applied to the converter equivalent circuit, using the method of the complementary tree, according e.g. to [FLM05] and documented in detail in Appendix A.1. For the all-AC circuit in Figure 4.1a, a set of three mesh and one junction equation is required for the complete network description, which then yields

$$v_1 = v_{\mathrm{Cr}} + R_1 i_1 + L_{1\mathrm{tot}} \dot{i}_1 + v_{\mathrm{M}}, \tag{4.1}$$

$$v_{\mathrm{M}} = v_{\mathrm{Fe}} = R_{\mathrm{Fe}} i_{\mathrm{Fe}}, \tag{4.2}$$

$$i_{\mathrm{Fe}} = i_1 - i_{\mathrm{M}} - \frac{1}{n} i_2, \tag{4.3}$$

$$v_{\mathrm{M}} = nR_2 i_2 + nR_{\mathrm{L}} i_2 + nL_2 \dot{i}_2. \tag{4.4}$$

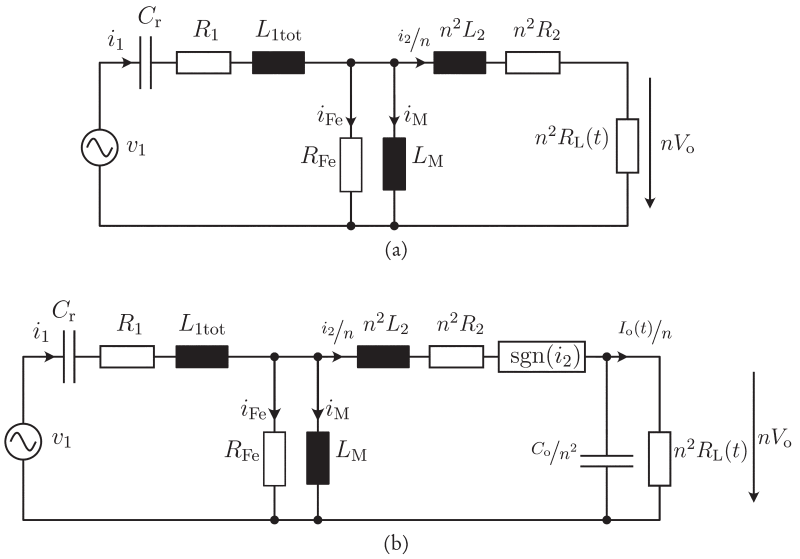


Figure 4.1.: Equivalent circuit diagram of a LLC resonance converter with nonlinear rectifier

The voltage drop on the resonance capacitor is v_{Cr} and that one on the transformer magnetizing inductance is v_{M}, which is equal to the transformer core loss voltage v_{Fe}. For the extended equivalent circuit from Figure 4.1b, equations (4.1 – 4.3) still hold true, equation (4.4) is reformulated and one additional junction is added to cover the additional grade of freedom from the DC output capacitor. Then, the additional equations

$$v_{\mathrm{M}} = nR_2 i_2 + nL_2 \dot{i}_2 + n\,\mathrm{sgn}(i_2) V_{\mathrm{o}}, \tag{4.5}$$

$$V_{\mathrm{o}} = \frac{1}{C_{\mathrm{o}}} \int i_{\mathrm{Co}}\,\mathrm{d}t, \tag{4.6}$$

$$i_2\,\mathrm{sgn}(i_2) = i_{\mathrm{Co}} + I_{\mathrm{o}}. \tag{4.7}$$

are obtained. With the set of equations(4.1 – 4.3, 4.5 – 4.7), the network is fully described and the state space model can be formulated. Due to the forward current conduction and reverse current blocking behavior of the rectifier diodes, the secondary side rectifier induces nonlinearity in form of the signum function with argument i_2 into the converters circuit equations (4.5, 4.7).

A Single Input Single Output (SISO) state space model with n independent energy storages has the general form

$$\dot{\boldsymbol{x}}(t) = \boldsymbol{A}\boldsymbol{x}(t) + \boldsymbol{b}u(t), \tag{4.8}$$

$$y(t) = \boldsymbol{c}^{\mathrm{T}}\boldsymbol{x}(t) + du(t), \tag{4.9}$$

where $\boldsymbol{b} \in \mathbb{R}^n$ is the model input vector, $\boldsymbol{A} \in \mathbb{R}^{n\times n}$ is the state matrix, $\boldsymbol{c}^{\mathrm{T}} \in \mathbb{R}^{1\times n}$ is the transposed output vector and $d \in \mathbb{R}$ is the systems transparency of its input $u \in \mathbb{R}$ versus the output $y \in \mathbb{R}$, the state vector is $\boldsymbol{x} \in \mathbb{R}^n$. Generally, a system featuring an output equation with non-zero transparency can cause an algebraic loop. Such systems are capable to immediately follow an input step excitation, which would imply a special risk of instability. Like for most systems, transparency vanishes for the system at hand and hence, the risk of an algebraic loop is not given.

For the all-AC circuit's state space system, the four state variables are chosen to be v_{Cr}, i_1, i_{M} and i_2. Accordingly, equations (4.1– 4.4) are reformulated, particularly (4.2– 4.4) yield

$$\dot{i}_2 = \frac{R_{\mathrm{Fe}}}{nL_2}i_1 - \frac{R_{\mathrm{Fe}}}{nL_2}i_{\mathrm{M}} - \frac{R_{\mathrm{Fe}} + n^2R_2 + n^2R_{\mathrm{L}}}{n^2L_2}i_2 \tag{4.10}$$

for the secondary current's deviation. This leads to the SISO state space system

$$\begin{pmatrix} \dot{v}_{\mathrm{Cr}} \\ \dot{i}_1 \\ \dot{i}_{\mathrm{M}} \\ \dot{i}_2 \end{pmatrix} = \begin{pmatrix} 0 & \frac{1}{C_{\mathrm{r}}} & 0 & 0 \\ -\frac{1}{L_{1\mathrm{tot}}} & -\frac{R_1+R_{\mathrm{Fe}}}{L_{1\mathrm{tot}}} & \frac{R_{\mathrm{Fe}}}{L_{1\mathrm{tot}}} & \frac{R_{\mathrm{Fe}}}{nL_{1\mathrm{tot}}} \\ 0 & \frac{R_{\mathrm{Fe}}}{L_{\mathrm{M}}} & -\frac{R_{\mathrm{Fe}}}{L_{\mathrm{M}}} & -\frac{R_{\mathrm{Fe}}}{nL_{\mathrm{M}}} \\ 0 & \frac{R_{\mathrm{Fe}}}{nL_2} & -\frac{R_{\mathrm{Fe}}}{nL_2} & -\frac{R_{\mathrm{Fe}}+n^2R_2+n^2R_{\mathrm{L}}}{n^2L_2} \end{pmatrix} \begin{pmatrix} v_{\mathrm{Cr}} \\ i_1 \\ i_{\mathrm{M}} \\ i_2 \end{pmatrix} \tag{4.11}$$

$$V_{\mathrm{o}} = \begin{pmatrix} 0 & 0 & 0 & \frac{1}{R_{\mathrm{L}}} \end{pmatrix} \begin{pmatrix} v_{\mathrm{Cr}} \\ i_1 \\ i_{\mathrm{M}} \\ i_2 \end{pmatrix}. \tag{4.12}$$

For the extended circuit with DC output sub-circuit, equations (4.1– 4.3, 4.5– 4.7) are utilized to describe the system dynamics. The state space system is formulated with the state variables of the all-AC system (4.11 – 4.12) and additionally V_{o} for the fifth state variable. With $I_{\mathrm{o}} = {}^{V_{\mathrm{o}}}/_{R_{\mathrm{L}}}$ and equations (4.6 – 4.7), the systems fifth equation (e.g., derivative of V_{o}) yields

$$\dot{V}_{\mathrm{o}} = \frac{1}{C_{\mathrm{o}}}\operatorname{sgn}(i_2)i_2 - \frac{1}{R_{\mathrm{L}}C_{\mathrm{o}}}V_{\mathrm{o}} \tag{4.13}$$

and equation 4.10 is reformulated to

$$\dot{i}_2 = \frac{R_{\mathrm{Fe}}}{nL_2} i_1 - \frac{R_{\mathrm{Fe}}}{nL_2} i_{\mathrm{M}} - \frac{R_{\mathrm{Fe}} + n^2 R_2}{n^2 L_2} i_2 - \frac{\operatorname{sgn}(i_2)}{L_2} V_{\mathrm{o}}. \tag{4.14}$$

Then, the converters state space system can be reformulated to

$$\begin{aligned}
\begin{pmatrix} \dot{v}_{\mathrm{Cr}} \\ \dot{i}_1 \\ \dot{i}_{\mathrm{M}} \\ \dot{i}_2 \\ \dot{V}_{\mathrm{o}} \end{pmatrix} &= \begin{pmatrix} 0 & \frac{1}{C_{\mathrm{r}}} & 0 & 0 & 0 \\ -\frac{1}{L_{1\mathrm{tot}}} & -\frac{R_1+R_{\mathrm{Fe}}}{L_{1\mathrm{tot}}} & \frac{R_{\mathrm{Fe}}}{L_{1\mathrm{tot}}} & \frac{R_{\mathrm{Fe}}}{nL_{1\mathrm{tot}}} & 0 \\ 0 & \frac{R_{\mathrm{Fe}}}{L_{\mathrm{M}}} & -\frac{R_{\mathrm{Fe}}}{L_{\mathrm{M}}} & -\frac{R_{\mathrm{Fe}}}{nL_{\mathrm{M}}} & 0 \\ 0 & \frac{R_{\mathrm{Fe}}}{nL_2} & -\frac{R_{\mathrm{Fe}}}{nL_2} & -\frac{R_{\mathrm{Fe}}+n^2R_2}{n^2L_2} & -\frac{\operatorname{sgn}(i_2)}{L_2} \\ 0 & 0 & 0 & \frac{\operatorname{sgn}(i_2)}{C_{\mathrm{o}}} & -\frac{1}{R_{\mathrm{L}}C_{\mathrm{o}}} \end{pmatrix} \begin{pmatrix} v_{\mathrm{Cr}} \\ i_1 \\ i_{\mathrm{M}} \\ i_2 \\ V_{\mathrm{o}} \end{pmatrix} \\
&\quad + \begin{pmatrix} 0 \\ \frac{1}{L_{1\mathrm{tot}}} \\ 0 \\ 0 \\ 0 \end{pmatrix} v_1
\end{aligned} \tag{4.15}$$

$$V_{\mathrm{o}} = \begin{pmatrix} 0 & 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} v_{\mathrm{Cr}} \\ i_1 \\ i_{\mathrm{M}} \\ i_2 \\ V_{\mathrm{o}} \end{pmatrix}. \tag{4.16}$$

This state space system has one input v_1, the only output is the voltage V_{o}, hence it has the form of a SISO system where the in- and output matrices are reduced to vectors. The nonlinearity from equations (4.5) and (4.7) reappears in the state matrix entries a_{45} and a_{54}, that link the secondary AC current i_2 to the DC output voltage V_{o}. With the signum function's solution, which is the finite set of $\{-1, 0, 1\}$, the converters state space model is no longer LTI, but is represented by a finite set of LTI state matrices, that represent the different solutions of the discrete function – in this case the signum function. This leads to a *switched linear system*, that is introduced in Section 2.5, with a set of state matrices $\boldsymbol{A}_{\sigma(t)}$ and a switching rule function $\sigma(t) \in \mathbb{M}$, that determines the active state matrix. For the problem at hand, the switching rule function is the sigma of i_2, yielding

$$\sigma(t) = \operatorname{sgn}(i_2(t)) \quad \in \mathbb{M}, \tag{4.17}$$

where $\mathbb{M} = \{-1, 0, 1\}$. The according entries in the state matrix attain the σ-dependent values

$$a_{45} = \begin{cases} -1/L_2 & i_2 > 0 \\ 0 & i_2 = 0 \\ 1/L_2 & i_2 < 0 \end{cases}, \tag{4.18}$$

$$a_{54} = \begin{cases} 1/C_\mathrm{o} & i_2 > 0 \\ 0 & i_2 = 0 \\ -1/C_\mathrm{o} & i_2 < 0 \end{cases} \tag{4.19}$$

respectively. Then, the system switches between the three linear state matrices, $\boldsymbol{A}_1$, $\boldsymbol{A}_0$ and $\boldsymbol{A}_{-1}$, for positive, zero and negative i_2, respectively, yielding the state matrix set $\boldsymbol{A}_{\sigma(t)} = \{\boldsymbol{A}_{-1}, \boldsymbol{A}_0, \boldsymbol{A}_1\} \in \mathbb{R}^{n \times n}$ for the switched linear system description of the problem at hand. During converter operation, the system switches between these three states with the alternation of i_2.

The physical effect, causing the switching behavior is the forward current conduction versus reverse current blocking behavior of the rectifier. The rectifier is fed by the current i_2, which represents a system state (namely x_4), hence according to Section 2.5, the system can be classified as state-dependent switched linear system. For the system's stability analysis, methods for state switched systems and systems under arbitrary switching can be applied. The later represent a more general system classification, rendering the analysis more conservative, e.g., the likeliness of finding a solution is lower. On the other hand, the solving algorithms are more robust in numerical computation.

The above established model (4.15 – 4.16) along with its classification as state-dependent switched linear system under arbitrary switching is the basis for the following system analysis and controller synthetization.

4.1.3. Model Analysis

For the controller design, a linear model of the converter's power circuit would be favorable applying the well-established methods of linear network analyses and controller synthesization. Since no linear model is at hand, options for controller synthesis are limited. For the system analysis, the converter model's subsystems will be investigated, applying classic methods as eigenvalue analysis, observability and

controllability analysis. The switched linear system is investigated for stability, using Lyapunov's Direct Method.

Fundamental to all work with numeric models (e.g., simulation or model-based control techniques) are stable numerical properties of the regarding model. One way to measure a systems numerical stability is the computation of the condition number of its state matrix $\boldsymbol{A}$ with $\mathrm{cond}(\boldsymbol{A}) \geq 1$. It is a measure of the distance of the inverse state matrix to singularity, for matrix conditions close to unity, the matrix is considered well-conditioned and numerical effects are insignificant. With the inverse getting closer to singularity, the condition increases, then the matrix is bad or ill-conditioned. If the inverse matrix is close to singularity, the equations solutions relative error caused from numerical rounding errors becomes large versus the input error. The effect on the numeric simulation of an initial value problem is the need for small simulation step size to achieve convergence of the computational error, which is necessary for accurate simulation result. The necessary simulation step size reduction increases the computational effort, the consequence for on line model computation is the need for high computational power. [Mei15, Ch. 2.3] The test of the all-AC and the DC-output circuit system matrices condition is part of the model analysis.

In the following both, the all-AC LTI model and the switched linear model with output DC circuit will be analyzed, starting with the all-AC model, followed by the switched linear model. Both models are parametrized with the physical quantities for the scaled model from the exemplary application in Section 3.4 with $25\,\mathrm{W}$ nominal power and $55\,\mathrm{V}$ to $70\,\mathrm{V}$ in- and output voltage per module (see Table A.2 in the Appendix for the complete parametrization).

The all-AC systems condition, rank, controllability and observability are symbolically computed, followed by numeric evaluation of the condition with the parametrization from Table A.2 under different converter loads, the results are as follows:

$$\begin{aligned}
\mathrm{cond}(\boldsymbol{A}) &= \begin{cases} 47 \cdot 10^9 & \text{for } P = 1\,\mathrm{W} \\ 1.9 \cdot 10^9 & \text{for } P = 25\,\mathrm{W} \end{cases} \\
\mathrm{rank}(\boldsymbol{A}) &= 4 \\
\mathrm{rank}(\boldsymbol{S}_\mathrm{S}) &= 4 \\
\mathrm{rank}(\boldsymbol{S}_\mathrm{B}) &= 4,
\end{aligned}$$

where $\boldsymbol{S}_\mathrm{S}$ is the system's controllability matrix and $\boldsymbol{S}_\mathrm{B}$ is the systems observability matrix. With given condition above 10^9, the simulation of the system requires high computational effort and numeric evaluations are afflicted with significant uncertainties. Due to the systems bad condition, the systems poles and zeros are computed symbolically, using a computer algebra software and the results are evaluated with

Table 4.1.: System Characteristics for the all-AC system

Poles		*Damping Frequencies*	*Resonance*	*Zeros*
$s_1 =$	$-3642 \cdot 10^3$ $P = 1\,\mathrm{W}$	1	580 kHz	
	$-870 \cdot 10^3$ $P = 5\,\mathrm{W}$		138 kHz	
	$-184 \cdot 10^3$ $P = 10\,\mathrm{W}$		29.3 kHz	
	$-88.4 \cdot 10^3$ $P = 15\,\mathrm{W}$		14.1 kHz	
	$-57.4 \cdot 10^3$ $P = 20\,\mathrm{W}$		9.1 kHz	
	$-42.9 \cdot 10^3$ $P = 25\,\mathrm{W}$		6.8 kHz	
$s_{2,3} =$	$(-15.3 \pm \mathrm{j}161) \cdot 10^3$ $P = 1\,\mathrm{W}$	$95 \cdot 10^{-3}$	25.7 kHz	$\{0, 0\}$
	$(-61.6 \pm \mathrm{j}160) \cdot 10^3$ $P = 5\,\mathrm{W}$	$359 \cdot 10^{-3}$	27.3 kHz	
	$(-168 \pm \mathrm{j}216) \cdot 10^3$ $P = 10\,\mathrm{W}$	$613 \cdot 10^{-3}$	43.5 kHz	
	$(-132 \pm \mathrm{j}309) \cdot 10^3$ $P = 15\,\mathrm{W}$	$392 \cdot 10^{-3}$	53.5 kHz	
	$(-104 \pm \mathrm{j}337) \cdot 10^3$ $P = 20\,\mathrm{W}$	$296 \cdot 10^{-3}$	56.1 kHz	
	$(-85.4 \pm \mathrm{j}349) \cdot 10^3$ $P = 25\,\mathrm{W}$	$238 \cdot 10^{-3}$	57.2 kHz	
$s_4 =$	$-677 \cdot 10^6$ $P = 1\,\mathrm{W}$	1	108 MHz	
	$-501 \cdot 10^6$ $P = 5\,\mathrm{W}$		79.7 MHz	
	$-479 \cdot 10^6$ $P = 10\,\mathrm{W}$		76.5 MHz	
	$-472 \cdot 10^6$ $P = 15\,\mathrm{W}$		75.1 MHz	
	$-468 \cdot 10^6$ $P = 20\,\mathrm{W}$		74.5 MHz	
	$-466 \cdot 10^6$ $P = 25\,\mathrm{W}$		74.1 MHz	

the system parameters to gain accurate numerical values. The system matrix is fully ranked; hence the system has no linear dependent lines and rows, $\mathrm{rank}(\boldsymbol{A})$ is equal to the number of independent energy storages in the circuit from Figure 4.1a. Also, the controllability and observability matrices are fully ranked, indicating that all states are controllable and observable.

The characteristics of the all-AC system are stated in Table 4.1. All eigenvectors and eigenvalues are load dependent and are seated in the closed left half of the Laplace plane for the designs load spectrum. The first and the fourth pole are real and the pole pair $s_{2,3}$ is complex with load-variable damping, it represents the converter's load dependent resonance behavior. The system's transfer function, as defined in (4.15 –

4.16) has a load independent double zero in the origin.
With the poles in the left half plane, the system matrix is Hurwitz, hence state stability is given. The double zero in the origin yields a double pole in the same location for the control loop, closed with a P-controller. Then the closed loop's poles are located in the left half plane plus an additional double pole in the origin, hence closed loop input/output stability is given, while state stability is not guaranteed due to the double pole in the origin. [Lun14, Ch. 8]

The switched linear system model's condition, rank of the system, controllability and observability matrices are computed equally to the ones for the all-AC LTI system for each $\sigma(t)$, it yields:

$$\begin{aligned}
\mathrm{cond}(\boldsymbol{A}_{\sigma(t)}) &= 2.3 \cdot 10^6 && \text{for } \sigma(t) = \pm 1 \\
\mathrm{cond}(\boldsymbol{A}_{\sigma(t)}) &= 2.3 \cdot 10^7 && \text{for } \sigma(t) = 0 \\
\mathrm{rank}(\boldsymbol{A}_{\sigma(t)}) &= 5 && \forall\ \sigma(t) \\
\mathrm{rank}(\boldsymbol{S}_{\mathrm{S}}) &= 5 && \forall\ \sigma(t) \\
\mathrm{rank}(\boldsymbol{S}_{\mathrm{B}}) &= 5 && \forall\ \sigma(t).
\end{aligned}$$

The load dependency of the condition of the state matrix $\boldsymbol{A}_{\sigma(t)}$ is insignificant. For $\sigma(t) = \pm 1$, the condition is equal, while it is one decade larger for $\sigma(t) = 0$. Compared to the all-AC system, the switched linear system's condition is smaller by approx. two decades, but still badly conditioned with poor expected numerical computation performance, especially real time computing can be expected to be challenging.
All three system matrices are fully ranked; hence, all five independent energy storages are represented in the state space model. All three subsystems are fully controllable and observable if investigated separately. Unfortunately, switched linear systems, consisting only of controllable/observable subsystems can lose these properties by certain switching sequences. Hence switching must be included in the controllability/observability analysis of switched systems [SG05, Ch. 4].

A method to investigate a discrete-time switched linear system on observability and controllability is published by Egerstedt and Babaali [EB05], by Trenn et. all. in [TT10] for observability and [KRT15] for controllability. Confidence over observability and controllability is mandatory for model predictive control methods. Anticipating the converter control strategies, presented in Section 4.2, such strategies are not applied within this work, primarily due to the system model's bad conditioning and the therefrom resulting challenges in the controller real time application. Without the mandatory need of this system characteristics for the applied control method, this rather challenging analysis is not exercised within this work. Nevertheless, this

shall point towards a future work topic, where more advanced controllers may be investigated on the presented converter system.

Table 4.2.: System Characteristics for system matrices $\boldsymbol{A}_1$, $\boldsymbol{A}_{-1}$ and $\boldsymbol{A}_0$

Matrices: $\boldsymbol{A}_1$, $\boldsymbol{A}_{-1}$				
Poles		*Damping*	*Resonance Frequencies*	*Zeros*
$s_{1,2} =$	$-47.1 \pm \mathrm{j}6.69 \cdot 10^3$ $P = 1\,\mathrm{W}$	$7 \cdot 10^{-3}$	1 kHz	$\{0, 0\}$
	$-134 \pm \mathrm{j}6.69 \cdot 10^3$ $P = 5\,\mathrm{W}$	$20 \cdot 10^{-3}$		
	$-242 \pm \mathrm{j}6.69 \cdot 10^3$ $P = 10\,\mathrm{W}$	$36 \cdot 10^{-3}$		
	$-351 \pm \mathrm{j}6.68 \cdot 10^3$ $P = 15\,\mathrm{W}$	$52 \cdot 10^{-3}$		
	$-459 \pm \mathrm{j}6.68 \cdot 10^3$ $P = 20\,\mathrm{W}$	$69 \cdot 10^{-3}$		
	$-567 \pm \mathrm{j}6.67 \cdot 10^3$ $P = 25\,\mathrm{W}$	$85 \cdot 10^{-3}$		
$s_{3,4} = -92 \pm \mathrm{j}639 \cdot 10^3$		$0.25 \cdot 10^{-3}$	58.8 kHz	
$s_5 = -457 \cdot 10^6$		1	72.7 MHz	
Matrix: $\boldsymbol{A}_0$				
Poles		*Damping*	*Resonance Frequencies*	*Zeros*
$s_1 = -29.5$		1	4.69 Hz	
$s_2 =$	-43.4 $P = 1\,\mathrm{W}$	1	6.91 Hz	$\mathbb{C}$
	-217 $P = 5\,\mathrm{W}$		34.6 Hz	
	-434 $P = 10\,\mathrm{W}$		69.1 Hz	
	-651 $P = 15\,\mathrm{W}$		104 Hz	
	-868 $P = 20\,\mathrm{W}$		138 Hz	
	$-1.09 \cdot 10^3$ $P = 25\,\mathrm{W}$		173 Hz	
$s_{3,4} = -92 \pm \mathrm{j}639 \cdot 10^3$		$0.25 \cdot 10^{-3}$	58.8 kHz	
$s_5 = -457 \cdot 10^6$		1	72.7 MHz	

The characteristics for the switched linear system (4.15 – 4.16) are given in Table 4.2, the system matrices $\boldsymbol{A}_1$ and $\boldsymbol{A}_{-1}$ share identical characteristics and are given in the first part of the Table, while the characteristics for $\boldsymbol{A}_0$ are given in the lower part of the Table.
For $\boldsymbol{A}_1$, $\boldsymbol{A}_{-1}$, the pair of poles $s_{1,2}$ is load dependent, while the resulting resonance

frequency is constant with accuracy well above $1\,\%$, hence, resonance is load independent, while the damping of the according eigenvector pair increases with increasing load. The deviation of all three resonance frequencies, if computed at various loads lies well above $1\,\%$, hence they are considered load independent, they are $1\,\mathrm{kHz}$, $58.8\,\mathrm{kHz}$ and $72.7\,\mathrm{MHz}$ respectively. The system's transfer function, as defined in (4.15 – 4.16) has a load independent double zero in the origin – equal to the all-AC system.
For $\boldsymbol{A}_0$, the pole pair $s_{1,2}$ resolves to a constant real pole s_1 and a real pole s_2 with load dependent, increasing eigenfrequency. Pole pair $s_{3,4}$ and the pole s_5 are equal to the ones for $\boldsymbol{A}_1$ and $\boldsymbol{A}_{-1}$, hence they are independent from $\sigma(t)$. The subsystem's transfer function is $G_{\sigma(t)=0}(\mathrm{s}) = 0\ \forall \mathrm{s} \in \mathbb{C}$ for $\boldsymbol{A}_0$, hence the subsystems single zero is the complete s-plane. With the complete s-plane, the zero lies in the right half plane and a system with non-minimum phase behavior is achieved. The state $\sigma(t) = 0$ refers to the physical property, that no current flows from the converter's secondary AC circuit trough the rectifier into the DC output circuit, which means, that no output is generated from the input excitation – no signal transfer takes place. Without signal transfer, the control error in a closed-control loop will not decrease from control output, which can lead e.g., to run away of states, linked to the input or integrator windup over longer periods. This behavior occurs at operation frequencies f_{sw} below resonance in the time interval t_1 – t_2 (see Figure 2.10b). If this state occurs, the converter operates on the rising slope of the gain curves; preferentially avoiding this operational state.

According to the foregoing analysis, all three subsystems $\boldsymbol{A}_1$, $\boldsymbol{A}_{-1}$ and $\boldsymbol{A}_0$ are Hurwitz on their own and the necessary condition for input/output stability for switched linear systems is met. For switched linear systems, it is not sufficient to investigate the eigenvalues of the isolated subsystems for qualified statements about system stability. Under arbitrary switching, even a switched system's states with only stable LTI subsystems can diverge due to unfortunate switching sequences [LM99]. Therefore, Lyapunov's stability analysis is applied on the system under investigation. Roughly, it says that if an equilibrium point $\boldsymbol{x}_{\mathrm{e}}$ with an attraction area exists, and the system decays within finite time towards the equilibrium point for all initial states $\boldsymbol{x}_0 \in \mathbb{D}^n$ within the attraction area, then the system is asymptotically stable within $\mathbb{D}^n$ and if $\mathbb{D}^n = \mathbb{R}^n$, the system is globally, asymptotically stable. For the subsystems of the system at hand, the equilibrium points

$$\boldsymbol{x}_{\mathrm{e}1} = \boldsymbol{x}_{\mathrm{e}} = 0 \qquad \text{if } R_2 + R_{\mathrm{L}} \neq 0 \wedge R_{\mathrm{Fe}} \neq 0 \tag{4.20}$$

$$\boldsymbol{x}_{\mathrm{e}2} = \begin{pmatrix} 0 & 0 & z & \sigma(t)^{z_1/R_{\mathrm{L}}} & z_1 \end{pmatrix}^{\mathrm{T}} \qquad \text{if } R_2 + R_{\mathrm{L}} = 0 \wedge R_{\mathrm{Fe}} = 0 \wedge \sigma \neq 0 \tag{4.21}$$

$$\boldsymbol{x}_{\mathrm{e}3} = \begin{pmatrix} 0 & 0 & -\sigma(t)^{z}/_{nR_{\mathrm{L}}} & \sigma(t)^{z}/_{R_{\mathrm{L}}} & z \end{pmatrix}^{\mathrm{T}} \quad \text{if } R_2 + R_{\mathrm{L}} = 0 \wedge R_{\mathrm{Fe}} \neq 0 \wedge \sigma \neq 0 \tag{4.22}$$

$$\boldsymbol{x}_{\mathrm{e}4} = \begin{pmatrix} 0 & 0 & z & 0 & 0 \end{pmatrix}^{\mathrm{T}} \quad \text{if } R_2 + R_{\mathrm{L}} \neq 0 \wedge R_{\mathrm{Fe}} = 0 \neq 0 \wedge \sigma \neq 0 \tag{4.23}$$

$$\boldsymbol{x}_{\mathrm{e}5} = \begin{pmatrix} 0 & 0 & z & z_1 & 0 \end{pmatrix}^{\mathrm{T}} \quad \text{if } R_2 = 0 \wedge R_{\mathrm{Fe}} = 0 \wedge \sigma = 0 \tag{4.24}$$

$$\boldsymbol{x}_{\mathrm{e}6} = \begin{pmatrix} 0 & 0 & -z/n & z & 0 \end{pmatrix}^{\mathrm{T}} \quad \text{if } R_2 = 0 \wedge R_{\mathrm{Fe}} \neq 0 \wedge \sigma = 0 \tag{4.25}$$

$$\boldsymbol{x}_{\mathrm{e}7} = \begin{pmatrix} 0 & 0 & z & 0 & 0 \end{pmatrix}^{\mathrm{T}} \quad \text{if } R_2 \neq 0 \wedge R_{\mathrm{Fe}} = 0 \wedge \sigma = 0 \tag{4.26}$$

are obtained. The constraints for the equilibrium points are resistor values of some of the resistors in the converter model. As resistor values, they are never negative or zero. With these system constraints, only the constraints from (4.20) are met, and are met for all possible valid systems, while the constrains of the remaining equilibrium points are never met – most of them due to zero values, where a positive value is expected. In conclusion, the system has one single equilibrium point in the origin, that is valid for all three subsystems.

With known equilibrium point, the switched linear converter model (4.15 – 4.16) is investigated for stability with a CQLF, the converter is parametrized according to Table 4.2, the initial time is set $t_0 = 0$ without loss of generality. The Lyapunov Function is investigated under aid of computer numeric software with and without preconditioning, investigation details are given in Appendix A.2. The CQLF without preconditioning yields the symmetrical matrix and its determinants

$$\boldsymbol{P} = \begin{pmatrix} 3.11 \cdot 10^{-17} & 2.83 \cdot 10^{-18} & -5.19 \cdot 10^{-18} & -1.73 \cdot 10^{-18} & 1.71 \cdot 10^{-22} \\ 2.83 \cdot 10^{-18} & 1.19 \cdot 10^{-12} & -1.91 \cdot 10^{-13} & -2.68 \cdot 10^{-13} & 2.95 \cdot 10^{-19} \\ -5.19 \cdot 10^{-18} & -1.91 \cdot 10^{-13} & 5.29 \cdot 10^{-12} & 2.67 \cdot 10^{-13} & -2.82 \cdot 10^{-19} \\ -1.73 \cdot 10^{-18} & -2.67 \cdot 10^{-13} & 2.67 \cdot 10^{-13} & 4.20 \cdot 10^{-13} & -3.94 \cdot 10^{-19} \\ 1.70 \cdot 10^{-22} & 2.95 \cdot 10^{-19} & -2.82 \cdot 10^{-19} & -3.94 \cdot 10^{-19} & 4.60 \cdot 10^{-15} \end{pmatrix}$$

$$\begin{aligned} \det \boldsymbol{P}_1 &= 3.111 \cdot 10^{-17} \\ \det \boldsymbol{P}_2 &= 3.6995 \cdot 10^{-29} \\ \det \boldsymbol{P}_3 &= 1.9476 \cdot 10^{-40} \\ \det \boldsymbol{P}_4 &= 6.8263 \cdot 10^{-53} \\ \det \boldsymbol{P}_5 &= 3.144 \cdot 10^{-67}, \end{aligned}$$

where the determinants of the matrices' determinants with indices $i = \{1 \dots 5\}$ represent the submatrices $\boldsymbol{P}_i \in \mathbb{R}^{i \times i}$. Hence, for the tested CQLF, $\boldsymbol{P}$ is positive definite. Due to the submatrices small distance to zero, the CQLF is tested with preconditioned system matrices $\boldsymbol{A}_{\sigma(t)}$, yielding

$$\boldsymbol{P} = \begin{pmatrix} 1.04 \cdot 10^{-16} & 1.15 \cdot 10^{-19} & -1.98 \cdot 10^{-16} & -5.38 \cdot 10^{-18} & -5.66 \cdot 10^{-24} \\ 1.15 \cdot 10^{-19} & 2.37 \cdot 10^{-12} & 2.21 \cdot 10^{-12} & 2.49 \cdot 10^{-13} & -8.43 \cdot 10^{-20} \\ -1.98 \cdot 10^{-16} & 2.21 \cdot 10^{-12} & 9.87 \cdot 10^{-12} & -3.90 \cdot 10^{-13} & 1.75 \cdot 10^{-19} \\ -5.38 \cdot 10^{-18} & 2.49 \cdot 10^{-13} & -3.90 \cdot 10^{-13} & 7.66 \cdot 10^{-14} & 2.00 \cdot 10^{-20} \\ -5.66 \cdot 10^{-24} & -8.43 \cdot 10^{-20} & 1.75 \cdot 10^{-19} & 2.00 \cdot 10^{-20} & 1.27 \cdot 10^{-14} \end{pmatrix}$$

$$\begin{aligned} \det \boldsymbol{P}_{\mathbf{1}} &= 1.049 \cdot 10^{-16} \\ \det \boldsymbol{P}_{\mathbf{2}} &= 2.494 \cdot 10^{-28} \\ \det \boldsymbol{P}_{\mathbf{3}} &= 1.9465 \cdot 10^{-39} \\ \det \boldsymbol{P}_{\mathbf{4}} &= 1.3401 \cdot 10^{-54} \\ \det \boldsymbol{P}_{\mathbf{5}} &= 1.7114 \cdot 10^{-68}. \end{aligned}$$

Preconditioning gains little improvement for the first three determinants and even falls back below the results of the unconditioned state matrices for the fourth and fifth determinant. Even though the determinants of $\boldsymbol{P}$ are close to zero for both cases, with and without preconditioning, the CQLFs for both cases yield positive definite matrices $\boldsymbol{P}$ for the problem at hand and with given parametrization, detailed results are documented in the Appendix A.2. The (sub-) determinants of $\boldsymbol{P}$ are close to zero but acceptably far away for the utilized computer system. Hence, $\boldsymbol{P}$ is symmetrical positive definite and with this matrix properties, it is proven that a CQLF exists for the linear switched converter model. With the existing CQLF, it is proven, that the LLC converter is globally asymptotically stable, hence disturbances settle in finite time.

4.2. Control Strategies for Converter Modules

The control strategy for the DC/DC converter comprises two major functionalities. First, the voltage stabilization at nominal voltage during converter operation. This control task guaranties the power delivery to the connected electrical loads by compensating voltage drops e.g., due to increasing load. Voltage stabilization also protects converter and connected consumers from potentially destructive over voltage. Second,

the controller contains a startup routine, which controls the secondary voltage rise and the power flow from the primary to the secondary side to avoid voltage overshoot and over current, that may lead from live-shortening component stress up to destruction. Over-current and voltage overshoots are primarily caused by the uncharged DC output filter capacitor, in the turn on instance of the converter, it's impedance is low and hence high current rushes into it, followed by a voltage overshot from the high current. A simple solution to avoid the described phenomenon during startup is the implementation of pre-charge circuits, where the output circuit's impedance is increased during capacitor charging by series connection of a pre-charge resistor for the sake of power loss. When the load current has dropped below a predefined value or after a certain time interval, the pre-charge resistor is shortened. A more sophisticated method to limit the inrush current is the limitation of the input voltage gradient by a soft start routine, as it will be implemented here. In the following sections, the focus lies on the voltage stabilization, the startup routine is addressed in Section 4.2.1.

4.2.1. Startup Routine for Controlled Output DC Capacitor Charging

Generally speaking, DC/DC converter startup includes the complete process from power down of all circuits over the powering of all necessary auxiliary circuits as driver, measurement and controller circuits. All these circuits are required to be ready to operate before the actual converter circuit that transfers the electrical energy is initially activated. This phase ends when the converter has reached its dedicated output voltage and is ready for power transmission. Narrowing down the view in this work, startup references the process from where all auxiliary circuits are ready to operate and the turn-on of the power transmission is triggered in any form to the point, when the converter is ready for power transmission.
In the introduction to this Chapter, the specific challenges in the charging of the output DC filtering capacitor are sketched out. The state-of-the-art solution to this issue is the hardware implementation of a precharge circuit, where the charging current is limited by a resistor series connected to the capacitor. To overcome the disadvantage of such an energy dissipative setup with precharge capacitor, a controlled startup can be utilized by a so-called soft start routine, where the initial voltage rise follows a trajectory towards the nominal setpoint in a way, that the inrushing capacitor current remains in a non-hazardous range. Soft start routines are discussed in recent literature e.g., in [FL14].

In the startup situation, the converter's control circuit is referenced by a trajectory, to steer the output to the nominal output voltage. It is designed in a way, that the

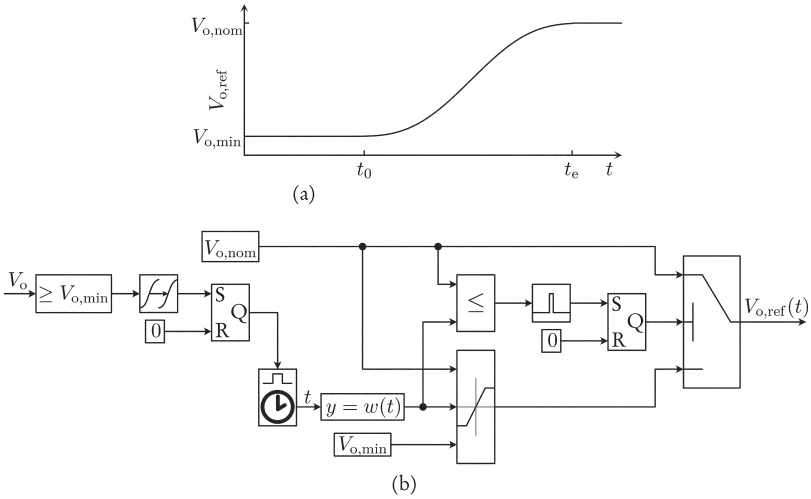


Figure 4.2.: Voltage-reference trajectory during converter startup in part (a) and online generation of the output voltage reference including startup trajectory in part (b).

converter's controller is capable to dynamically follow its course, ideally without deviation and without overshoot. The concept to obtain such a trajectory is presented in [Lun14, Ch. 7], it is based on the system's zero and internal dynamics, that are obtained from a state-space model transformation, its fundamentals are presented in Subsection 2.4.1 of this work. The trajectory's shape solely relies on the control system's relative grade, further constraints as value limitation of particular state variables are not considered. If such constraints exist – e.g., secondary current limitation – they must be validated in an iterative process, for example by simulation. The method from [Lun14, Ch. 7] requires that for a control variable trajectory with continuously differentiable characteristic, the according actuating value trajectory is also continuously differentiable. In the LLC converter transfer behavior from the actuating value f_{sw} to the control variable V_o, continuous differentiability is not fully given. One point of discontinuity exists between the turned-off state and the standard operation mode: When the converter is turned off, naturally no actuating value is generated, hence, it is equals zero: $f_{sw} = 0\,\text{Hz}$. Steering the output voltage steadily from converter turn-off state towards nominal voltage would lead over the positive slope and the maximum peak of the gain characteristics. Since, the positive slope does not represent an allowed converter operating range and the peak eventually causes hazardous output voltage,

the actuating value must jump to the characteristic's allowed negative slope, causing a point of discontinuity in the actuator value trajectory for startup.

The fundamental startup strategy smoothly steers the converter output voltage from turn-off condition to the dedicated voltage setpoint $V_{\mathrm{o,ref}} = V_{\mathrm{o,nom}}$ without unnecessary voltage or current stress by specification of an appropriate reference voltage trajectory. Based on the technique from Subsection 2.4.1, aim is to initially activate the controller with its maximal operating frequency and subsequently steer the output voltage to nominal voltage with a reference voltage trajectory. The initial activation at maximal operating frequency is achieved by initially referencing the minimum converter output voltage at given load $V_{\mathrm{o,ref}} = V_{\mathrm{o,min}}$ either by computing or experimentally acquiring this working point. The control structure – introduced later in this chapter – must be designed in a way that the controller output to the initial voltage reference value is the maximum operating frequency $f_{\mathrm{sw,max}}$. Once, V_{o} has reached $V_{\mathrm{o,min}}$, the trajectory is activated to steer V_{o} to its steady state value, where it remains for the remaining operating time. The complete startup trajectory is plotted in Figure 4.2a. From the system characteristics in Table 4.2, we have five poles and one double zero, hence the relative grade is $r = 5 - 2 = 3$, which yields $p = 2r + 1 = 2 \cdot 3 + 1 = 7$ for the polynomial in the form of equation (2.28) in the Figure. The specific polynomials parametrization for the problem at hand is documented in Appendix A.3. The reference generation method with the soft-start voltage trajectory is depicted in Figure 4.2b. The soft start is activated, when $V_{\mathrm{o}} \geq V_{\mathrm{o,min}}$ is satisfied for a given time delay, this will trigger the activation latch on the figure's left side. The activation of the latch marks the time instance t_0, where the reference voltage transition starts. This is implemented by the initiation of the time reference for the trajectory function by the latch output. The reverence value from the trajectory polynomial is subsequently conditioned by a saturation block, with lower limitation to $V_{\mathrm{o,min}}$ and upper limitation to $V_{\mathrm{o,ref}}$ and a switching unit that switches the voltage reference to constant $V_{\mathrm{o,ref}}$, once, $w(t) \geq V_{\mathrm{o,ref}}$. The later constraint is implemented since $w(t)$ falls below $V_{\mathrm{o,ref}}$ with progressing runtime.

With the output voltage trajectory at hand and the corresponding trajectory generation algorithm, the converter voltage controller can be provided with an appropriate voltage signal to ensure converter soft start without overly high component stress. This voltage trajectory will be utilized as reference signal to the voltage controller and will be introduced in the following subsections.

Table 4.3.: Performance requirements for the LLC-converter control task.

Rise Time	*exact*
Delay Time	*exact*
Max. Voltage Overshoot	$5\,\%$
Max. Voltage Sag due to Load Change	$-5\,\%$
Static Voltage Accuracy	$\pm 1\,\%$

4.2.2. Conception of the Fundamental Controller Structure for the Converter Module

In this chapter's first section, the LLC converter is mathematically modeled for theoretical analysis regarding its dynamic behavior, stability and numerical characteristics. The mathematical approach yielded a switched linear system with three state matrices. The switching depends on the rectifier's diode current. Analysis in Subsection 4.1.3, with regard to numeric properties, showed that the matrices are ill conditioned, which leads to high computational effort to achieve accurate results when computing a converter model. This computational effort may be acceptable during offline computing, where computation time is not crucial but becomes challenging if the model is computed online, e.g., for MPC or state observers and computational results must be present in real-time within a given (short) time range. In conclusion, recognizing the foregoing sections, it can be stated that most advanced control techniques are not applicable to the problem at hand and a controller with less computational effort is favorable. Therefore, a controller shall be utilized, where the computational effort remains reasonable, with still good control properties. Good control properties are defined in Table 4.3. As the following details describe, such a controller structure consists of a PID controller with superposed feed forward switching frequency computation from the converter's inverted characteristic curve set.

Figure 4.3 gives an overview over the chosen controller concept of the DC/DC converter. The controller concept includes a combination of a linear PID controller with a feed forward control. The open loop feed forward control computes an operating switching frequency value f_{ff} for the inverter from an output voltage reference value $V_{\mathrm{o,ref}}$ and measurable disturbances, that are input voltage V_{in} and converter output current I_{o}. System dynamics are not included within the f_{ff} computation to achieve reasonable computing load. Additionally, the minimal switching frequency at current load $f_{\mathrm{sw,min}}(P_{\mathrm{Load}})$ is provided by the feed forward control – this value must not be deseeded at any time during operation to prevent loss of zvs. The remaining control error e, on one hand caused from system dynamics and on the other hand

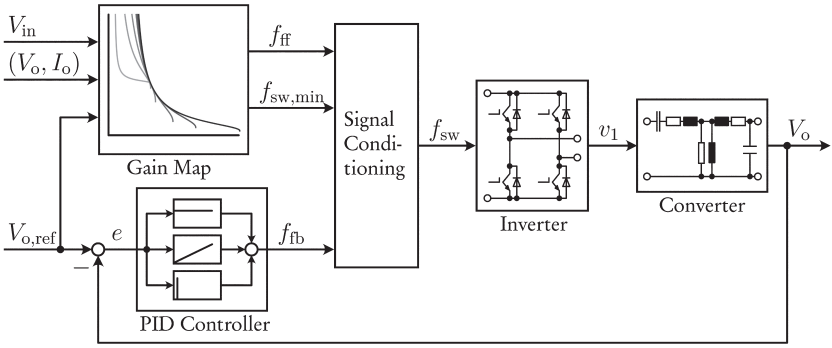


Figure 4.3.: Signal diagram of a controlled DC/DC converter with feed forward control and linear PID feedback control

from uncertainties in the feed forward controller model. Unmeasurable disturbances are compensated by the linear closed loop feedback control. The frequency signals from the feed forward and feedback controller, f_{ff} and f_{fb} respectively, are summed and conditioned in the signal conditioning entity, its output is the inverter switching frequency f_{sw} within the signal limits $f_{\mathrm{sw,min}}(P_{\mathrm{Load}})$ and $f_{\mathrm{sw,max}}$. The inverter generates the rectangular, bipolar voltage excitation v_1 for the converter circuit from the feeding DC voltage V_{in}. The fundamental frequency of v_1 is the inverter's switching frequency f_{sw} and its amplitude is equal to the feeding DC voltage V_{in}. The inverter's dynamics are considered negligible, hence the transmission function from f_{sw} to v_1 is purely algebraic. The actual control system is the LLC converter with resonance circuit, transformer, rectifier and DC output circuit as modeled in Section 4.1. It is driven by the rectangular voltage v_1, its output is the problem's control variable V_{o}. The control strategy's sub functionalities and their implementation are detailed in the following subsections.

4.2.3. Feed Forward Control

In the feed forward controller, the converter switching frequency is extracted from a characteristic diagram, it is funded on the converter stationary DC to DC gain function FHA model (2.9 – 2.26) from Section 2.3.2. The diagram is implemented in form of a 3-D lookup table with input variables converter gain M and load equivalent resistance R_{L}. For increased accuracy, the FHA converter model from Subsection 2.3.2 is extended by the dissipative losses R_1, R_2 and R_{Fe} from the transformer equivalent

model, as well as the transformer primary and secondary leakage inductances L_1 and L_2. The full extended FHA model's equivalent circuit is according to Figure 4.1a. For the converter gain $M_{\mathrm{fha,ext}}$, the modified gain function yields

$$\begin{aligned} M_{\mathrm{fha,ext}}(f_\mathrm{n}, R_\mathrm{e}) &= \left| \frac{Z_\mathrm{o}}{Z_\mathrm{tot}} \right| \\ &= \left| \frac{A_0^\mathrm{N} + f_\mathrm{n}^2 A_2^\mathrm{N} + \mathrm{j}\left(f_\mathrm{n} B_1^\mathrm{N} + f_\mathrm{n}^3 B_3^\mathrm{N}\right)}{f_\mathrm{n} A_1^\mathrm{D} + f_\mathrm{n}^3 A_3^\mathrm{D} + \mathrm{j}\left(-B_0^\mathrm{D} + f_\mathrm{n}^2 B_2^\mathrm{D} + f_\mathrm{n}^4 B_4^\mathrm{D}\right)} \right|, \end{aligned} \tag{4.27}$$

with the coefficients

$$A_0^\mathrm{N} = R_\mathrm{Fe}^2 R_\mathrm{e}\left(n^2 R_2 + R_\mathrm{e}\right) \tag{4.28}$$

$$A_2^\mathrm{N} = \frac{1}{L_\mathrm{1tot} C_\mathrm{r}} L_\mathrm{M}^2 R_\mathrm{e}\left(n^2 R_2 - R_\mathrm{Fe} + R_\mathrm{e}\right) \tag{4.29}$$

$$B_1^\mathrm{N} = \frac{1}{\sqrt{L_\mathrm{1tot} C_\mathrm{r}}} R_\mathrm{e} R_\mathrm{Fe}^2\left(L_\mathrm{M} + n^2 L_2\right) \tag{4.30}$$

$$B_3^\mathrm{N} = \frac{1}{L_\mathrm{1tot} C_\mathrm{r}} \frac{1}{\sqrt{L_\mathrm{1tot} C_\mathrm{r}}} L_\mathrm{M}^2 n^2 L_2 \tag{4.31}$$

$$A_1^\mathrm{D} = \sqrt{\frac{C_\mathrm{r}}{L_\mathrm{1tot}}} R_1 R_\mathrm{Fe}^2\left(n^2 R_2 + R_\mathrm{e}\right) + \frac{1}{\sqrt{L_\mathrm{1tot} C_\mathrm{r}}} R_\mathrm{Fe}^2\left(L_\mathrm{M} + n^2 L_2\right) \tag{4.32}$$

$$\begin{aligned} A_3^\mathrm{D} = \frac{1}{\sqrt{L_\mathrm{1tot} C_\mathrm{r}}} \Bigg(& \frac{L_\mathrm{M}^2}{L_\mathrm{1tot}} \left(R_1\left(n^2 R_2 + R_\mathrm{e} - R_\mathrm{Fe}\right) - R_\mathrm{Fe}\left(n^2 R_2 + R_\mathrm{e}\right)\right) \\ & - R_\mathrm{Fe}^2 \left(L_\mathrm{M}\left(n^2 \frac{L_2}{L_\mathrm{1tot}} + 1\right) + n^2 L_2\right)\Bigg) \end{aligned} \tag{4.33}$$

$$B_0^\mathrm{D} = -R_\mathrm{Fe}^2\left(n^2 R_2 + R_\mathrm{e}\right) \tag{4.34}$$

$$\begin{aligned} B_2^\mathrm{D} = \frac{1}{L_\mathrm{1tot}} \Bigg(& R_\mathrm{Fe}^2\left(\left(L_\mathrm{1tot} L_\mathrm{M}\right)\left(n^2 R_2 + R_\mathrm{e}\right) + R_1\left(L_\mathrm{M} + n^2 L_2\right)\right) \\ & - \frac{L_\mathrm{M}^2}{C_\mathrm{r}}\left(n^2\left(R_2 + L_2\right) + R_\mathrm{e} - R_\mathrm{Fe}\right)\Bigg) \end{aligned} \tag{4.35}$$

$$B_4^{\mathrm{D}} = \frac{L_{\mathrm{M}}^2}{L_{1\mathrm{tot}} C_{\mathrm{r}}} \left(n^2 \left(\frac{L_2}{L_{1\mathrm{tot}}} R_1 R_2 + L_2 - \frac{L_{\mathrm{M}} L_2}{L_{1\mathrm{tot}}} R_{\mathrm{Fe}} \right) + R_{\mathrm{e}} - R_{\mathrm{Fe}} \right). \tag{4.36}$$

For the detailed derivation of the gain function refer to Appendix A.4. Here, the resistive and – more significant – the inductive, internal voltage loss of the transformer is included in the model.
With the extended gain function, a gain chart is computed and the gain, or respectively the load to frequency characteristic is obtained according to the procedure according to Figure 4.4. In the first preparing step, the vectors $\boldsymbol{f}_{\mathrm{n}} \in \mathbb{R}^k$ and $\boldsymbol{r}_{\mathrm{e}} \in \mathbb{R}^l$ with equidistant frequency, respectively load equivalent values are generated. The frequency vector ranges from the designed overall minimum to the maximum converter switching frequency, the resistor vector is set to cover a reasonable range of partial load and over load, i.e., $\boldsymbol{r}_{\mathrm{e}} = R_{\mathrm{L}} \cdot (0.01, \ldots, 2)^T$. With these input data, the gain matrix $\boldsymbol{M}_{\mathrm{fha,ext}}(\boldsymbol{f}_{\mathrm{n}}, \boldsymbol{r}_{\mathrm{e}}) \in \mathbb{R}^{l \times k}$ from the extended FHA model (4.27) is computed in step two. Since the converter's permitted operating region is limited to the negative slope of the gain function – e.g., right of the maximal gain, in the matrix' each column the maximal gain value is searched. The load dependent frequency values, that correspond to the column wise maximum gain positions in the matrix represent the load dependent minimum converter frequencies and are stored in the vector $\boldsymbol{f}_{\mathrm{sw,min}}(R_{\mathrm{e}}) \in \mathbb{R}^l$. In the gain matrix, all entries left of the gain maxima are removed.
Subsequently, the gain values are harmonized to equidistance. Therefore, the equidistant vector $\boldsymbol{m}_{\mathrm{fha,ext}} = [\min(\boldsymbol{M}_{\mathrm{fha,ext}}), \ldots, \max(\boldsymbol{M}_{\mathrm{fha,ext}})] \in \mathbb{R}^k$ is created and the according frequencies are column-wise spline interpolated. The spline interpolation's results are written to the lookup table breakpoint matrix $\boldsymbol{F}_{\mathrm{n}} \in \mathbb{R}^{k \times l}$.
The vector $\boldsymbol{f}_{\mathrm{sw,min}}(R_{\mathrm{e}})$ with the load dependent minimum switching frequencies is implemented in a characteristic curve and returns the current minimum converter switching frequency to the control for bounding the command signal from bottom.

Within this controller block, the lockup tables input signals are the desired converter gain $M_{\mathrm{ref}} = {}^{V_{\mathrm{o,ref}}}/_{2n^2 V_{\mathrm{in}}}$. The load equivalent resistance $R_{\mathrm{e}} = {}^{8V_{\mathrm{o}}}/_{(\pi^2 I_{\mathrm{o}})}$ is achieved from measurable values by online preprocessing. For the converter gain, additional corrections are necessary since the FHA model on which the lookup table is based computes with AC values, whereas for the converter control DC in and output values are of interest. To satisfy this, the gain reference is computed under consideration of the voltage loss in the primary side inverter and the secondary side rectifier, hence the gain reference can be found

$$M_{\mathrm{ref}} = \frac{V_{\mathrm{o,ref}} + 2V_{\mathrm{df}} + 2R_{\mathrm{df}} I_{\mathrm{o}}}{2n^2 \left(V_{\mathrm{in}} - (2V_{\mathrm{on}} + R_{\mathrm{on}} n I_{\mathrm{o}}) \right)}, \tag{4.37}$$

where $2V_{\mathrm{df}}$ is the voltage drop on the rectifier diode junctions and $2R_{\mathrm{df}} I_{\mathrm{o}}$ is the resistive voltage loss in the rectifier diodes. The input voltage is reduced by the IGBT

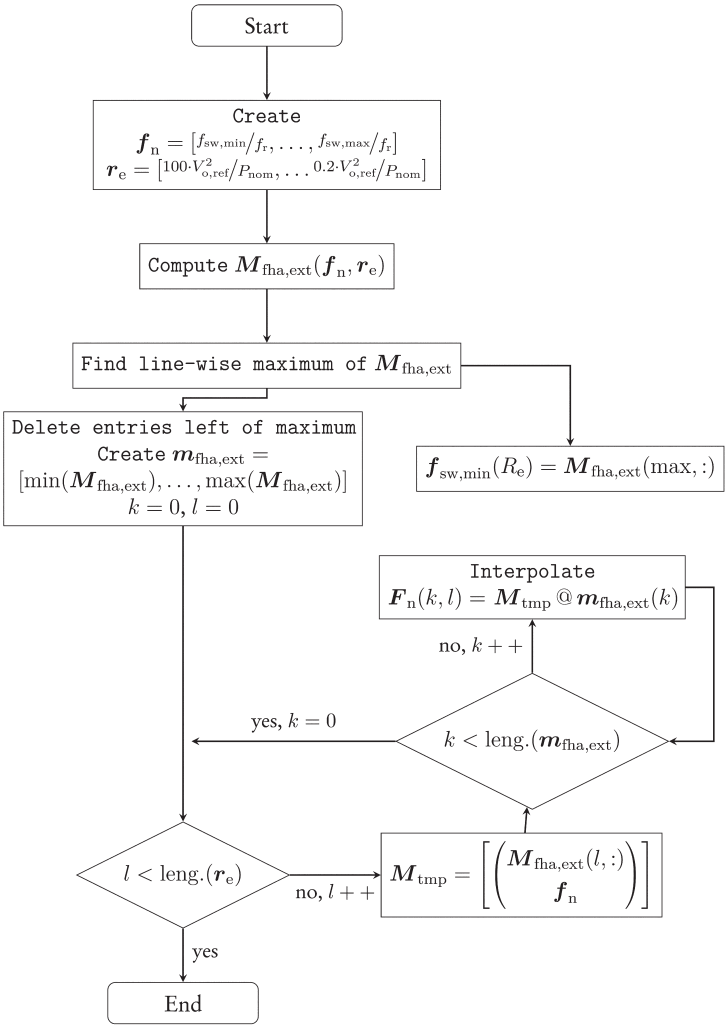


Figure 4.4.: Flowchart, depicting the post processing procedure for the gain/load to inverter switching frequency lookup table

junctions' voltage loss $2V_{\mathrm{on}}$ and the resistive loss $R_{\mathrm{on}}nI_{\mathrm{o}}$, which is approximated from the measured and primary side transformed DC output current. Consequently, besides the control reference, the measured converter primary side voltage and current – approximated by nI_{o} – effects the forward control result, so that primary side voltage disturbance and inverter voltage loss can be compensated to a good degree.
Since the feed forward model only relies on static values, the measured variables are low pass filtered with large filter time constant compared to the controller iteration frequency to block out instantaneous controller reactions with large amplitudes, that lead to undesirable oscillations.

4.2.4. Feedback Control

The feedback control operates parallel to the feed forward control. It improves the overall controller performance by compensation of errors, that cannot be corrected by the feed forward control, such as unmeasurable disturbances, model inaccuracies and dynamic effects. It is implemented in form of a linear PID controller with DC output voltage error input and inverter switching frequency correction signal as controller output signal. During startup, the PID controller is activated if the control error initially falls below the predefined threshold $|e \leq e_{\mathrm{act}}|$.
Since the converter model (4.15 – 4.16) is neither LTI nor linearizable in the working range, the extensive controller design methods for LTI systems cannot be applied for the controller parameter determination. Instead, the tuning is executed iteratively by simulating the converter model.

Due to the narrow bandwidth of the permissible inverter switching frequency, integrator windup may become a performance issue, which is commonly treated by anti-windup mechanisms. Typical mechanisms are to stop the integration if the integrator output exceeding the upper or lower actuator gain. In this application, the limits are dynamically computed as

$$f_{\mathrm{aw,min}} = f_{\mathrm{ff}} - f_{\mathrm{sw,max}} \leq 0 \tag{4.38}$$

for the integrator anti-windup upper limit (open loop feed forward frequency output f_{ff}, maximally allowed converter switching frequency $f_{\mathrm{sw,max}}$) and

$$f_{\mathrm{aw,max}} = f_{\mathrm{ff}} - f_{\mathrm{sw,min}}(P_{\mathrm{Load}}) \geq 0 \tag{4.39}$$

for the lower anti-windup cutoff frequency (minimal switching frequency at current load $f_{\mathrm{sw,min}}(P_{\mathrm{Load}})$).

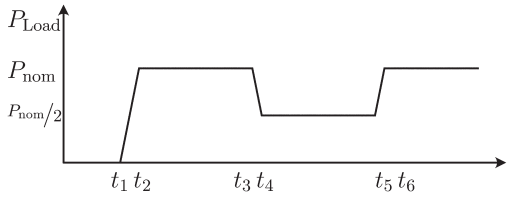


Figure 4.5.: Benchmark load profile for standardized controller performance tests

4.2.5. Signal Conditioning for the Combination of Feedback and Feedforward Control

In the *Signal Conditioning* block of the converter controller unit, the inverter switching frequency commands from the feed forward controller f_{ff} and the feedback controller f_{fb} are merged and conditioned. In the given control concept, the feed forward controller is the primary source of the command signal, the feedback controller generating a correction signal to compensate remaining control errors, it is subtracted from the feed forward command signal, since a decreasing of the switching frequency results in increased output voltage, while an increasing of the output voltage results in an increasing of f_{fb}.
In the next step, the command signal is limited to the permissible load-dependent operating space of the converter. The upper limit is defined by the semiconductors fast switching capability, usually the IGBTs are the crucial elements, this limit is operating state independent. The lower limit is dynamically adapted according to the converter's operating conditions with the aim to avoid loss of zvs. Therefore, the output signal of the 1-D lookup table from the feed forward controller generation containing the information $\boldsymbol{f}_{\mathrm{sw,min}}(R_{\mathrm{e}})$ is applied to the lower command signal limit. The complete signal conditioning can be expressed by

$$f_{\mathrm{sw}} = \min(\max(f_{\mathrm{ff}} - f_{\mathrm{fb}}, f_{\mathrm{sw,min}}(P_{\mathrm{Load}})), f_{\mathrm{sw,max}}). \tag{4.40}$$

4.2.6. Definition of a Benchmark Test for Dynamic Load Tests

A benchmark load profile is required to test the control performance, it is aimed to represent a broad variety of load states and various load changes within a reasonable time slot to give a good overview over controller performance. For this work the load profile from Figure 4.5 is defined for the standard benchmark test. The load profile starts in idle mode. During this time period the converter control executes its startup procedure, the startup behavior and idle performance can be evaluated. In the short

time interval $[t_1, t_2]$, the load rises to nominal power, the $^{dP}/_{dt} = {}^{P_{\mathrm{nom}}}/_{t_2 - t_1}$ should represent a typical current rise rate for a typical load in the load and voltage class of the given application. The load rise from t_1 to t_2 represents the largest possible load rise and covers the complete relevant frequency spectrum, it will provoke the largest overshoots and integrator windup. The next transition is executed in $[t_3, t_4]$, to half power, with equal $|^{dP}/_{dt}|$ as the first one, to analyze an abrupt load decline. In the following section, partial load behavior is modeled, with subsequent rise to full load in $[t_5, t_6]$. This benchmark load profile is used for all converter module and modular converter evaluations within this work.

4.3. Control Algorithm for a Modular DC/DC Converter

If a number of converter modules is connected to a combined modular converter, as presented in Section 3.1, an overall control concept is required. Apart from the stabilization of the over-all converter output voltage, in the modular converter a uniform voltage and power distribution between the converter modules is desired. In the following subsections, two major concepts are presented for the modular converter control for a parallel input – series output connected converter. The first concept relies on an individual module control, where each converter module is controlled by its own controller. The controller reference signal is coordinated by one common superordinate reference signal generation instance. The second concept comprises one global controller for all modules with control signal distribution to the individual converter modules. The general converter module setup for the following concept presentations is parallel input – series output terminal connection, if other setups are considered, it will be explicitly stated in the relevant text.

4.3.1. Individual Module Control for Modular DC/DC Converters

Figure 4.6 presents the basic structure of a modular DC/DC converter with individual module controllers. The voltage reference and the measurable disturbances are displayed in the Figures left center. These signals are distributed to and processed on module level, hence the voltage reference is scaled by the number of converter modules N to the module reference voltage ${}^{V_{\mathrm{o,ref}}}/_{N}$. The input voltage V_{in} and output current I_{o} are scaled with unity, due to the the parallel input – series output converter setup.

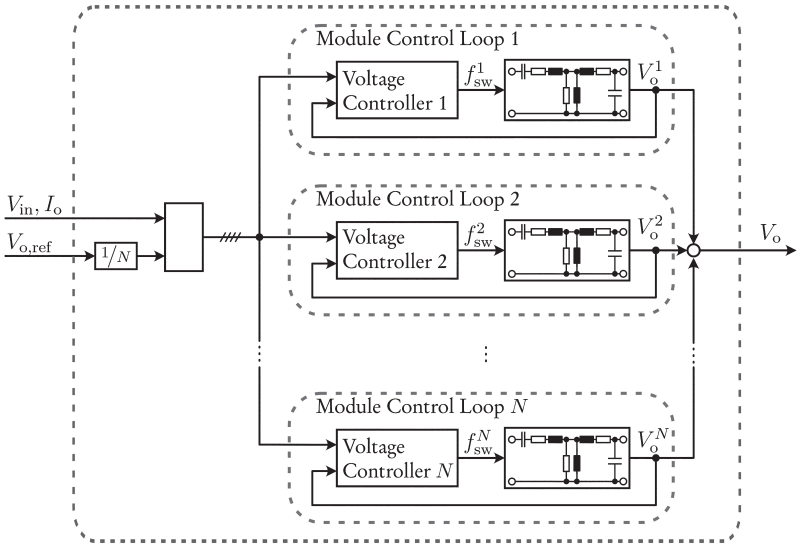


Figure 4.6.: Modular DC/DC converter control concept with independent voltage controllers for each module

In a series input setup, V_{in} and in parallel output, I_o is scaled by $1/N$, respectively. The complete scaling of the controller input signals for all permutations of the converter parallel/series and input/output setup is given in Table 4.4. The individual controllers of the modules 1 – N independently compute the switching frequency command signals f_{sw}^1 – f_{sw}^N. Their inner structure is according to Section 4.2.
The modules' control loops are closed by their output voltages V_o^1 – V_o^N without interfering with each other. The overall converter output voltage is gained by electrically summing up the module output voltages which is not fed back to the control loop. Hence the converter output voltage is only indirectly controlled by the control of the module output voltages.

In the control concept with individually controlled converter modules, the controller for the single module control from Section 4.2 is applied straight forward. The controllers of each module compensate device scattering and disturbances on module level, which leads to non-uniform switching frequencies f_{sw}^1 – f_{sw}^N. The voltage and power distribution relies on the input and output setup.
With output terminals connected in series, the output voltage is uniformly distributed over the modules. All modules are operated at their best point of operation, safety

Table 4.4.: Scaling of the controller input vector, according to the parallel/series, input/output permutations

Input – Output Setup	*Controller Input Vector*
parallel – parallel	$[V_{\mathrm{o,ref}},\ {}^{I_\mathrm{o}}/_{N},\ V_{\mathrm{in}}]$
parallel – serial	$[{}^{V_{\mathrm{o,ref}}}/_{N},\ I_\mathrm{o},\ V_{\mathrm{in}}]$
serial – parallel	$[V_{\mathrm{o,ref}},\ {}^{I_\mathrm{o}}/_{N},\ {}^{V_{\mathrm{in}}}/_{N}]$
serial – serial	$[V_{\mathrm{o,ref}},\ {}^{I_\mathrm{o}}/_{N},\ {}^{V_{\mathrm{in}}}/_{N}]$

margins in the module design can be kept as small as possible. On the downside, the overall voltage and current output ripples will be variable, due to overlaying of different frequency values and corresponding moving phases. Further, due to the absence of a supervising controller, the output voltage may be inaccurate, errors might not be fully compensated. The later can be overcome by introduction of an additional supervising controller with significantly smaller bandwidth than the module controllers that adjusts the module reference values to compensate remaining output voltage errors.

4.3.2. Global Control of Modular DC/DC Converters

In the control concept with one global voltage controller for all submodules, the converter modules are all controlled by one controller, that distributes the switching frequency signal to the N converter modules. This controller architecture is presented in Figure 4.7, the global voltage controller on the left side is set up according to the voltage controller concept for LLC converters in Section 4.2. In this control system setup, the control variable is the overall converter output voltage $V_\mathrm{o} = \sum_{k=1}^{N} V_\mathrm{o}^k$. The module's output voltages are implicitly controlled via the given additive dependencies to V_o.

In this setup, the controller reference variable and the feed forward control's measured disturbances are scaled according to Table 4.4, which is therewith similar to the scaling of the individual module controller concept from Subsection 4.3.1. With the global control concept and serial output configuration, the control variable V_o must be scaled from overall converter to module level by ${}^{1}/_{N}$, additionally to the scaling from the Table. The controller is parametrized for converter module level regulation, with equal feedback controller parametrization as for one module and a feed forward controller containing the inverse gain characteristic curve set of one converter module.

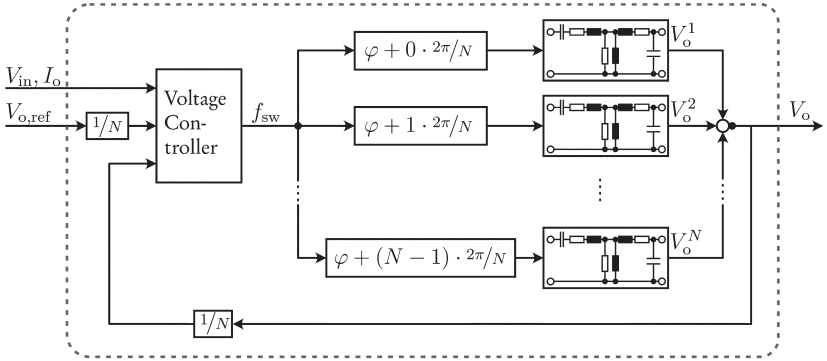


Figure 4.7.: Modular DC/DC converter with one superordinate voltage controller and phase shifted inverter drive signals for the modules

The command signal, computed by the controller is then distributed to the submodules according to the Figure, so that all submodules are driven with equal inverter switching frequency f_{sw}. With all converter modules being driven with equal switch frequency, all modules induce ripples with equal ripple frequency and amplitude on the output voltage during every instance of converter operation. This fact can be exploited for reduction of the overall voltage ripple on the converters output voltage by superposing the module ripples in a way, where maximal ripple compensation is achieved. For the compensation ripple superposition, the pulse pattern for the inverter operation is generated centrally in the voltage controller entity and distributed to the converter modules with phase delay $\varphi + (k-1) \cdot 2\pi/N, \forall\, k \in [1, \ldots, N]$ for the k^{th} module. This phase delay leads to an output voltage ripple frequency increased to $f_{\mathrm{ripple}} = N \cdot f_{\mathrm{r}}$ and a maximal ripple compensation. Theoretically, the compensation yields zero ripple for an even number of modules and increasing reduction for an increasing number of uneven modules. In praxis, an even number of modules will always display some remaining ripples due to physical effects as parameter variations or unequal signal traveling times to the module's inverters. Both effects, increased frequency and reduced output ripple, allow the utilization of smaller filtering capacitors to achieve equal ripple amplitude on the DC terminals.

In the global voltage controller mode, where the modules are operated with equal inverter frequency, the overall converter voltage is not uniformly distributed over the modules due to parameter scattering in the modules. With current sharing in the series connected output terminals, the module load distribution is proportional to the output voltage distribution. Hence, in the module design, additional safety margins

for voltage and load must be added to guaranty safe module operation. The effect of unequally distributed load and voltage to the converter modules is simulatively examined in the evaluation chapter.

5. Evaluation

The organization of this Chapter will guide the reader through the verification and evaluation process of the HV-DC/DC converter and the therefore designed voltage controller concept. Section 5.1 holds the proof of functionality of the hardware simulation models by means of key-waveform simulation and comparison versus theory from literature. In Section 5.2, the converter controller performance is evaluated for a single module and a modular converter by simulation means and the impact of converter parameter variation to the system is evaluated for a set of key parameters. Finally, in Section 5.3 the results of experimental tests featuring a scaled demonstrator are presented. This Section begins with the results of tests, that aim to proof the validity of the used simulation models from the experimental approach, followed by experiments with single modules and a modular converter setup.

The converter concepts, presented in Chapter 3, are modeled for numeric simulation with a computer numeric software package and an extension for physical modeling of power electronic circuits. In these models, the control laws from Chapter 4 are integrated for controller performance evaluation. With a further software extension for auto code generation and automated code uploading to a real time computing system, the controller parts of the simulation models are equipped for auto code generation for the following Hardware in the Loop (HIL) tests. The used simulation software package is a state-of-the-art tool for controller design tasks in academia as well as in the industry. In this Chapter it will be demonstrated, that simulations of power electronic circuits with this software are sufficiently precise for the application at hand. This software system is deliberately favored over Simulation Program with Integrated Circuit Emphasis (SPICE) software, which is the state of the art for electric circuit simulations. With SPICE, the electric circuit can certainly be simulated more precisely and time efficiently than under the used system, on the other hand, the tool chain for control design and the subsequent code generation and machine uplink is broken, making this process more challenging, hence, the chosen system presents a more integrated solution and is applied for this reason.

Table 5.1.: Simulation settings for the resonance circuit and rectifier diodes waveforms investigation.

Relation to f_r	Designated f_sw	Operating T_sw	Load R_L
At f_r	59.13 kHz	16.91 µs	196 Ω
Below f_r	44.99 kHz	22.2225 µs	1.96 kΩ
Above f_r	65 kHz	15.3825 µs	196 Ω

5.1. Converter Simulation Model Validation

Prior to the controller and HV converter modeling, the converter modules simulation model is validated. Therefore, it is analyzed towards its proper resonant switching behavior at, below and above switching frequency by comparing the switching behavior to the proposed waveforms as stated in the corresponding literature (given in Section 2.3). By comparing the resonance and the rectifier diode currents with respect to the semiconductor switching waveform versus the theoretical waveforms, the model and the simulation quality can be estimated. However, further analysis versus a prototype is necessary for validation and given later in this Chapter.

Table 5.1 gives the model settings for the simulation scenario at, below and above resonance frequency, respectively. The simulation is run at each of these settings to document the resonance circuit and rectifier diodes waveforms. It is set up, so that the model's inverter IGBTs are actuated with three different, dedicated constant switching frequencies f_sw to meet the three required operating states. According to the table, the converters output terminals are connected to a constant load resistor R_L. All three simulations are executed with the fixed time step size $T_\mathrm{s} = 2.5\,\mathrm{ns}$, until the DC output voltage is sufficiently settled. The inverse switching frequency $T_\mathrm{sw} = {}^1/_{f_\mathrm{sw}}$ is quantized by an integer multiple of the simulation step size T_s, hence values for T_sw given in Table 5.1 are exact values. From these values, f_sw is computed for the simulation parametrization. The actual plots for this section are generated from one period in the settled area of the recorded simulation results, the time axis' origin is corrected accordingly.

The simulated waveforms to study the converter switching behavior are given in Figure 5.1, where subfigures (a) and (b) show the results for simulation at resonance frequency f_r, subfigures (c), (d) below and (e), (e) above f_r. Subfigures (a), (c) and (e) represent a full switching period at given operating frequency and (b), (d) and (f) are detailed plots of the current commutation phase from positive to negative half wave. The first two plots in each subfigure represent the inverter IGBT actuation PWM

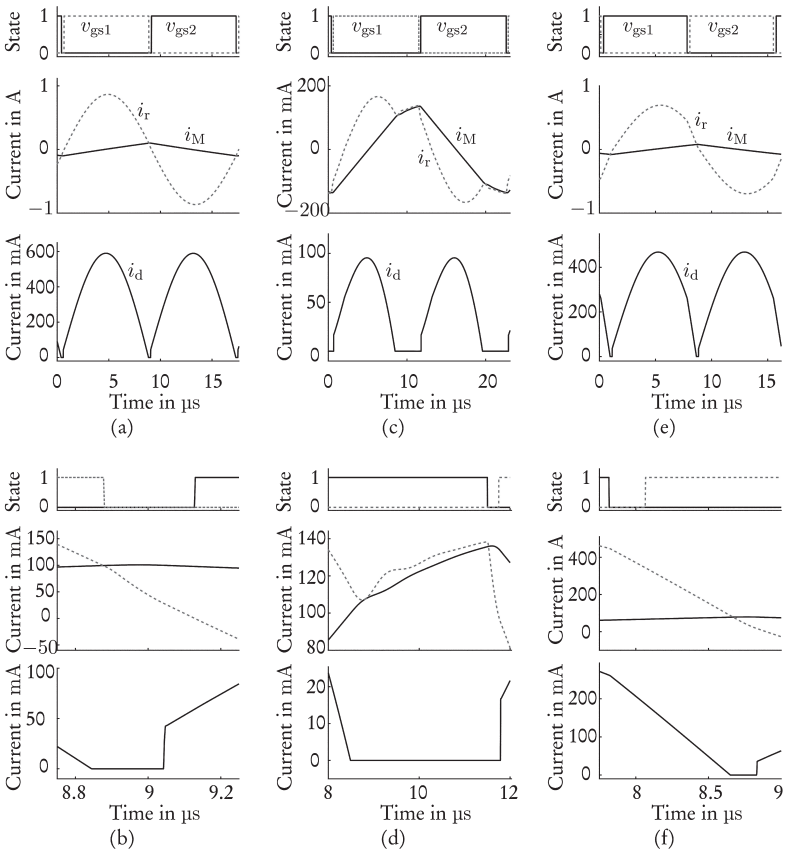


Figure 5.1.: Simulation of one period of the waveforms of the LLC full bridge converter model for operation (a) at, (c) below and (e) above resonance frequency f_r, respectively in the first row and the current commutation in the second row ((b), (d) and (f)).

signal, where 1 represents the IGBT on state and 0 the off state (e.g., proportional to v_{GS}) for referencing the simulated waveforms. Subsequently, the resonance circuit current i_r and the transformer magnetizing current i_M are plotted in one graph. On the figure's bottom graph, the full bridge rectifier output current is plotted, this

waveform represents the subsequent current through one (D_1, D_4) and the other (D_2, D_3) rectifier path.
In simulation at resonance frequency (subfigures (a), (b)), the resonance current describes a quasi-sinusoidal waveform, starting with the transition to conducting mode of IGBTs S_1 and S_4 and lasting over the IGBT-on period, while, at the same time, the transformer magnetizing current rises linearly. The falling resonance current roughly reaches the magnetizing current at approx. simulation time $t \approx 8.9\,\mu s$, where the corresponding IGBTs transition to off state. During the time interval in this first section, where i_r is positive and lies above i_M, the secondary side rectifier conducts through diode D_1 and D_4 and power is delivered to the load. As soon, as the resonance current reaches the magnetizing current, the secondary current reaches zero and hence, the power transfer is stopped. In the time interval of approx. $8.9\,\mu s \leq t \leq 9.15\,\mu s$, where all four IGBTs are turn-off – the inverter dead time, i_r rapidly drops towards zero, i_M still rises, but with lower gradient. Referring to the waveforms given in literature (and recited in Figure 2.10), i_r is expected to follow the magnetizing current until the later starts degrading. Instead, i_r continues degrading over the complete dead time. Since the secondary current is stopped at this time interval, the delta between resonance and magnetizing current in the corresponding knot (b in the complimentary tree in Figure A.1) is the current i_{Fe} flowing through the core loss equivalent resistance R_{Fe}. Core losses are widely ignored in the LLC converter waveforms given in the pertaining literature, hence the current wave form given here deviates from literature in this section. Shortly before i_r has fully dropped to zero, the complimentary IGBTs S_2 and S_3 are turned on. Due to the current direction in the resonance circuit, the current cannot conduct through the IGBTs and zcs is achieved – in this state, the current flows through the antiparallel diodes of S_2 and S_3. In the simulation, the secondary current flow through Diodes D_2 and D_3 roughly starts, when IGBTs S_2 and S_3 are tuned on and the waveform indicates a steep rise before continuing in quasi sinusoidal waveform, whereas the theoretical waveform has no edge when starting to conduct. This step is the result from the rectifier diodes modeled parasitic output capacitance c_{os}: When the – in this operation mode continuous – transformer output current changes sign, c_{os1} charges into c_{os3} and c_{os4} charges into c_{os2}. Once the output capacitors are charged, the current commutates on the antiparallel diodes and the output network is supplied with power. During commutation from negative to the positive half-period, the charging process executes vice versa.
The operating mode below resonance frequency (subfigures (c), (d)) is simulated as expected from theory, with the exception of the secondary side commutation. The resonance current describes the quasi-sinusoidal half wave until it hits the magnetizing current within the first half cycle at approx. $t \approx 9\,\mu s$. When i_M is reached, the secondary side current has reached zero and the diodes are softly turned off, subsequently i_r follows i_M until IGBTs S_1/S_4 are turned off. The commutation sequence is equal to the one, described here for operation at resonance frequency for the same reasons

and explanations – expect, the charge, stored inside the diodes parasitic capacitors is larger due to higher converter output voltage in this operating state.
The simulated converter behavior above resonance frequency is plotted in subfigures (e), (f). As expected, the resonance current lies well above i_{M} when the conducting converter IGBTs are turned off and the secondary current is non-zero. The following sharp degradation of resonance and secondary current is equal to the converter behavior in literature, the secondary side diode turn-on behavior is equal to their turn-on behavior at and below f_{r}.

In an overall perspective, all deviations from the theoretical waveforms of LLC converters described in literature are identified and are linked to specific physical properties of the simulation model at hand. Therewith it is shown, that the model represents the behavior of an LLC converter and is suitable for the following analyses of the converter behavior e.g., coupling of multiple converters and the controller design.
Limitations lie primarily in the roughly modeled semiconductors and lacking actuation circuits for the IGBTs, therewith investigation of the impact of various semiconductor technologies or efficiency evaluations are not feasible with the given model. The model validation versus a prototype demonstrator is still open and which will be presented in the experimental evaluation Section 5.3 of this chapter.

5.2. Simulative Evaluation of the Converter Control Concept

In this Section, the evaluation of the performance of the control strategies, developed in Sections 4.2 and 4.3 are investigated. This includes the soft-start routine developed in Section 4.2.1, where the converter output voltage is aimed to follow a reference trajectory to smoothly steer it towards the dedicated final output voltage with minimized voltage overshot and limited secondary side DC-capacitor inrush current. With results from a simulation run with one single converter module, the startup routine and the feed forward/feedback control law are evaluated. Simulation results from multi-module converter simulations are presented for the concept proof of the modular converter operation concept. For the controller evaluations in operational mode, the converter is operated with a load according to the benchmark test profile from Subsection 4.2.6 for the single module converter as well as for the modular converter. The model parametrization is implemented according to Appendix B.1. This section closes with a simulative analysis of parameter variations from a number

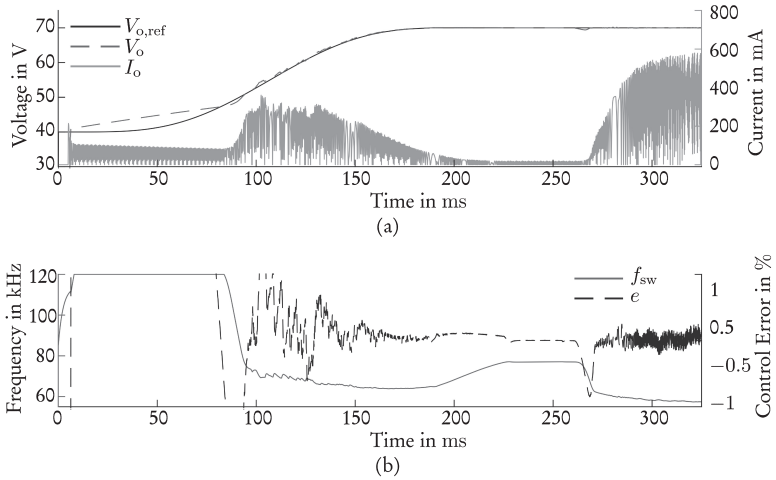


Figure 5.2.: Results from single module simulation of a controlled startup sequence with recorded time resolution of $100\,\mu s$ – (a): Simulated output voltage versus voltage reference on the left and output current on the right ordinate. (b): Converter actuating frequency f_{sw} on the left ordinate and output voltage control error in $\%$ on the right ordinate.

of model parameters to show the impact of such uncertainties to a modular converter setup and its operation.

5.2.1. Startup in Simulation

Figure 5.2 depicts a simulation run of a converter with one single module. In the time interval $t = [0, 200]\,\mathrm{ms}$, the converter startup routine according to Subsection 4.2.1 is recorded. Initially, the converter reference voltage is set to $V_{o,ref} = 40\,V$, which is the value, where the voltage rise under minimum converter gain with light load significantly slows down. Once, the output voltage reaches this initial reference, the reference describes the a priori computed trajectory to steer the converter output voltage to the nominal converter output voltage. After a short time interval to allow the output voltage to settle, the startup routine is finalized by lifting up the load power in the time interval $t = [500, 520]\,\mathrm{ms}$. During the startup procedure, the feedback

controller remains deactivated until the output voltage error drops below a defined value (here, it is set to 2 V) to avoid initial integrator windup.

Preliminary analysis was run, to determine where the converter output voltage rise is slowed down, when operated at the maximum operating frequency $f_{\mathrm{sw}} = 120\,\mathrm{kHz}$, started from off-state, where the converter is in its equilibrium state (e.g., $V_{\mathrm{o}} = 0\,\mathrm{V}$). With this setup, the converter rises towards $V_{\mathrm{o}} = 40\,\mathrm{V}$ within $1.4\,\mathrm{ms}$ and continues to rise a lot slower. Hence, the fed forward controllers voltage trajectory starts at $V_{\mathrm{o,ref}} = 40\,\mathrm{V}$, the respective reference trajectory, along with the according output voltage course are given on the left ordinate in Subfigure 5.2a, the corresponding rectifier output current is plotted versus the graphs right ordinate. At torn-on, the start-up controller sets the voltage reference constantly to $V_{\mathrm{o,ref}} = 40\,\mathrm{V}$ until V_{o} crosses the reference voltage and is held for 10 more controller cycles (e.g., $t = 1\,\mathrm{ms}$) to allow the V_{o}-rise to slow down in the vicinity of the trajectories start point. Subsequently, the reference trajectory transitions to the final output voltage setpoint of $V_{\mathrm{o,ref}} = 70\,\mathrm{V}$ by the fifth-order polynomial, presented in Subsection 4.2.1, and V_{o} follows with acceptable accuracy. Never the less, the control error is non-zero in the beginning, since V_{o} is not completely settled at the beginning of the final transition and has already risen above $40\,\mathrm{V}$, therefore, a short oscillation around $V_{\mathrm{o,ref}}$ is observed, which quickly settles. When reaching the final output voltage, no voltage overshot occurs. During this sequence, the converter's rectifier output current remains well below the converter's rectifier current under nominal load condition – which can be seen at around $t = 300\,\mathrm{ms}$, hence, the startup sequence effectively protects the converter from high inrush current, that present unintended stress to the device. Subsequently, the reference trajectory describes the fifth-order polynomial, which V_{o} is capable to follow exactly.
The converters operating frequency and the output voltage control error during this startup routine are given in Subfigure 5.2b on the left and right ordinate, respectively. The converter frequency shows the expected behavior, where it is operating at its maximum for the first few ms (here: approx. $90\,\mathrm{ms}$) and then softly drops in its range of normal operation, which is between approx. 55 – $80\,\mathrm{kHz}$. The control error graph shows, that the system has settled before it reaches its target voltage setpoint of $V_{\mathrm{o,ref}} = 70\,\mathrm{V}$.

5.2.2. Single Module Converter Control

With the gained confidence regarding the simulation models reliability, and the soft start concepts functionality confirmed by simulation, the controller concept is investigated next, by applying the load benchmark test according to Subsection 4.2.6 on the

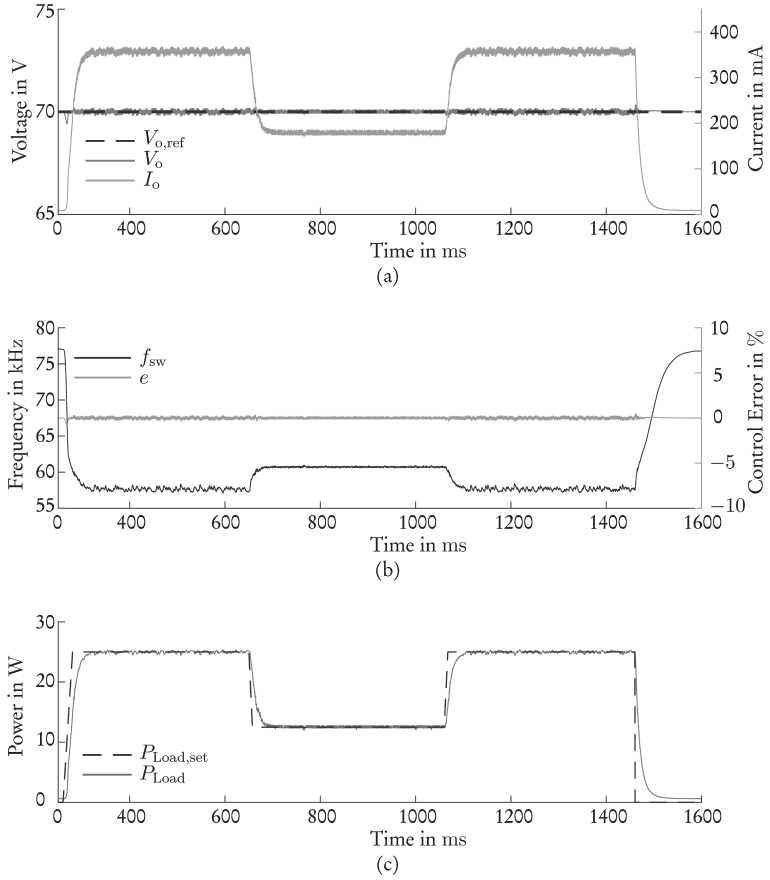


Figure 5.3.: Results from single module simulation of a controlled startup sequence with recorded time resolution of $100\,\mu s$: Subfigure (a) represents the simulated output voltage versus the voltage reference on the left and the output current on the right ordinate. In Subfigure (b), the converter actuating frequency f_{sw} on the left ordinate and the output voltage control error in % on the right ordinate are given. The actual load power and the set load is given in Subfigure (c).

converter in simulation. Again, the simulation model setup is configured according to Appendix B.1 and the converter voltage is stabilized at its nominal set-point, simulation results are given in Figure 5.3. In Subfigure 5.3a the converter output voltage during execution of the benchmark test is plotted versus its reference value against the left ordinate, visualizing the load current against the same graphs right ordinate. The converters operating frequency and the voltage control error are plotted versus the left and right ordinate of Subfigure 5.3b, respectively and the load set-point $P_{\mathrm{Load,set}}$ and actual converter load are given in Subfigure 5.3c.

Simulation results of the benchmark test show very stable output voltage behavior for full-load, half-load and idle load condition. The output voltage oscillation around the voltage reference shows proportionality to the load – though oscillation is generally small. When the load is initially ramped up from idle to full-load, a small voltage dip of as litle as $0.6\,\mathrm{V}$ can be observed, which is less than $-1\,\%$ deviation, the complete dip takes $10\,\mathrm{ms}$ from degrading from the set-point until V_{o} settles back again. The remaining load transitions between full- and half-load and from full-load to idle show no significance to the converters output voltage control. The converter switching frequency graph in Subfigure (b) depict the expected sequence of the control loops correcting variable. The load dynamics in Subfigure (c) are of subordinate significance, since the load emulation entity within the applied simulation model is modeled with slow dynamics to avoid instable feedback to the converter.

In conclusion, this section displays, that the converter control concept leads to stable converter operation under high and medium load and idle condition, as well as for load variations in various scales and both, positive and negative variations, showing a certain degree of robustness. Due to the slow load dynamics within the simulation model, precise statements with regard to the converters capability to stabilize high load dynamics are limited. With confidence of the well-functioning of the converter model – at least in simulation, the modular converters control performance for start-up and the benchmark test is investigated in the following subsection.

5.2.3. Modular Converter Control Simulation Results

In the present subsection, a modular converters dynamic behavior in setup, where the output voltage is regulated with one global controller according to Subsection 4.3.2 computes the switching frequencies for all converter modules, the module actuation signals are phase delayed against each other to achieve best elimination of output voltage ripples. For this simulation, a converter with three modules in input-parallel, output-serial configuration is simulated. Therefore, for once, the converter turn-on procedure is executed to steer the converters output voltage to nominal reference and

Table 5.2.: Parameter set for the investigation of the impact of parameter variation

Element	*Error Set*
–	$\{\pm 0\,\%\}$
C_r	$\{-25\,\%, +25\,\%\}$
L_M	$\{-50\,\%, +100\,\%\}$
C_o	$\{-25\,\%, +25\,\%\}$

subsequently, the benchmark test is applied to the converter. The simulation results are given in Figure 5.4 with a recording resolution of $1\,\mathrm{ms}$. In 5.4a, the converter output voltage reference $V_{\mathrm{o,ref}}$ and the actual output voltage V_o are plotted versus the left ordinate and the load current I_o is plotted on the right one. The load graphs are given in subfigure (c), converter switching frequency f_sw and the voltage control error on part (b) left and right ordinate, respectively and the modules' output voltages are given in (d).
The figure shows a simulation run from turn-on over the soft start routine, followed by a benchmark test after a short time gap to allow the converter to fully settle. The voltage reference in subfigure (a) represents the triple of the actual reference computed by the controller, since the controller computes the reference on module level but in the Figure, it is compared versus the converter output voltage.

In the startup phase, the converter shows equal behavior to the single module converter. Here, the reference starts at $40\,\mathrm{V}$ per module (e.g., $120\,\mathrm{V}$) and subsequently forms a trajectory towards the final reference voltage. The figure shows, that the output voltage quickly follows the reference and does not shoot over the final reference value. Again, the significant voltage error with a maximum of $10\,\%$ in the early phase of the startup routine is caused by the switching frequencies upper limitation at $120\,\mathrm{kHz}$. In the following benchmark test, the converter stabilizes the output voltage for every load and load change without any significant control error or deviation from the single module converters behavior. Over the complete simulation, all three converter module output voltages are overlying each other, showing no significant deviation.

The above shown simulation results lead to the conclusion that the converter concept, aligned with the presented control concept, delivers good dynamic performance. Further, the controller is able to stabilize the presented converter setup at least under ideal conditions of simulation with equal parametrization for all converter modules.

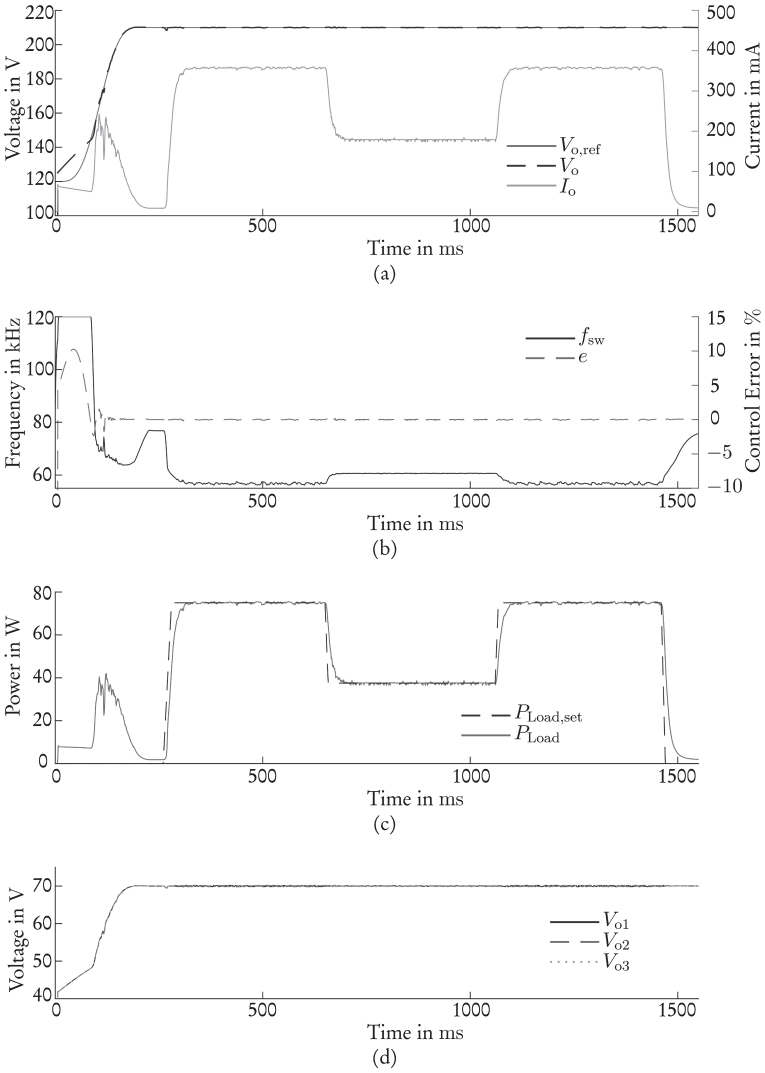


Figure 5.4.: Benchmark results from simulation with tree modules in parallel input, series output configuration and global controller approach. Subfigure (a): V_o vs. $V_{o,ref}$ on the left and I_o on the right ordinate. (b): Frequency f_{sw} vs. left and control error e vs. right ordinate. (c): Load P_{Load} and reference $P_{Load,set}$. (d): Output voltages of all three modules.

5.2.4. Impact Analysis of Parameter Variances on the Converter

Among others, tolerances e.g. in component manufacturing and individual aging behavior per component, result in slightly different converting behavior of each single converter module. In a DC/DC converter that consists of one converter module, the voltage control algorithm compensates such variances and hence, those are of minor interest, as long as they are kept within tolerable boundaries. Looking at the high voltage converter concept with serial or parallel connected converter modules and a proposed control concept where all modules are actuated with one single controller output, those above-described parameter variations become interesting for deeper analysis with respect to their impact on the overall system behavior.
For this analysis, key parameters of the converter module are identified and investigated by simulation. Parameter variances may occur e.g., from production or aging issues. For the tests, the key parameters are mistuned one by one to the negative and to the positive in one single module of a modular converter setup, while the remaining modules are held at their original design parametrization. As major key characteristics, the converter resonance frequency is manipulated and therewith the converter frequency-to-gain characteristics by right/left shifting. Alteration of the normalized inductance L_n results in changing steepness of the converters gain characteristics. Drifting capacitance of the series connected DC-capacitors may lead to shifting voltage distribution on the corresponding DC terminal and therewith to different power transfer of the various modules. The resonance frequency can be altered either by the resonance capacitor C_r or the resonance inductor L_r, L_n is affected either by L_r or L_M.
Derived from the foregoing reflection, the converter elements identified as suitable for investigation are the resonance capacitance C_r for alteration of resonance frequency, the transformer magnetizing inductances L_M to manipulate L_n and the capacitance in the capacitive voltage divider in a series connected converter side – as outlined in Table 5.2. For the magnetizing inductance, the influences are multiple and hence uncertainties are considered high. Hence, the converter model is investigated in a relatively wide error margin of $\{-50\,\%, +100\,\%\}$ for L_n. Anticipatory, it is said that variations of $\{-50\,\%, +100\,\%\}$ applied to the resonance capacitance lead to unreasonably extreme results, therefore, this parameter variation is set to $\pm 25\,\%$ for the investigation. The capacitive voltage divider structure can be implemented with standard out of stock components with good manufacturing accuracy. Hence the error margin is assumed to be smaller and is set to $\{-25\,\%, +25\,\%\}$ for the DC-capacitors.

For the impact analysis of parameter variances, the system model is set up with tree converter modules in parallel-input, series-output configuration. Two modules (Module 1 and Module 2) are parametrized with nominal values for all simulation

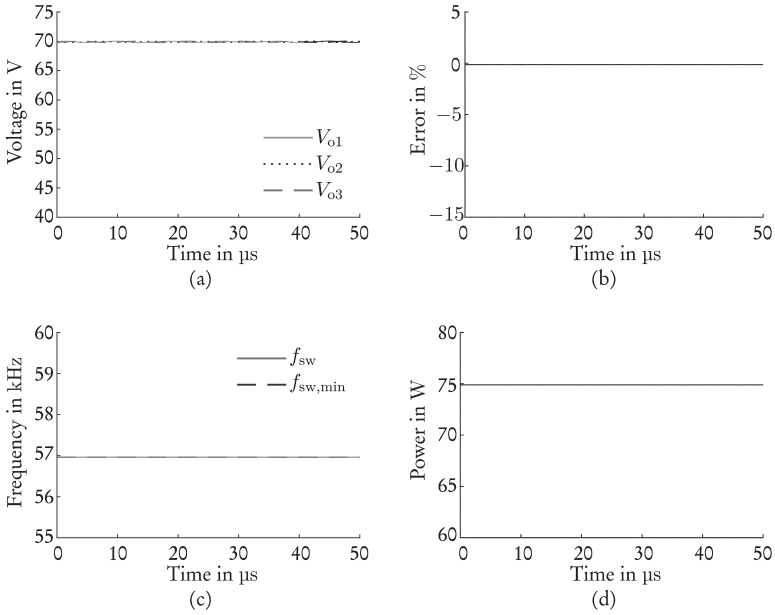


Figure 5.5.: Input-parallel, output-series connected converter setup with tree modules under reference simulation with nominal parametrization.

runs. In Module 3, the parameter variation is implemented as follows: For each evaluated parameter, two simulations are executed, the first parametrizes Module 3 with the estimated minimum worst case parameter deviation for the parameter under evaluation and the second run is parametrized with the parameters estimated maximum worst-case deviation in Module 3. For every parameter variation, the modular converter model is simulated once, therefore, a set of simulation results with one run per deviation is received. The complete set of simulations for this analysis is given in Table 5.2. In addition to the simulations with the worst-case parameter deviations, one reference simulation is executed without any deviation from the nominal converter parametrization in Module 1, Module 2 and Module 3. During the simulation runs, the modular converter is operated with applied output voltage control with the global control concept introduced in Subsection 4.3.2. The converter load is set to full load and a $50\,\mu s$ snapshot from the simulations steady state region is plotted.

Table 5.3.: Resonance frequency values for the LLC-converter with varied resonance frequency.

	Parameter Deviation Value		
	0 %	−25 %	+25 %
f_r	59.3 kHz	68.5 kHz	53.1 kHz
Frequency deviation from nominal	–	15.5 %	−10.5 %
f_r1	25.5 kHz	29.4 kHz	22.8 kHz
Frequency deviation from nominal	–	15.3 %	−10.6 %

Figure 5.5 shows the simulation results of the reference simulation with nominal converter parametrization. The module output voltages of all three converter modules are given in Subfigure (a), all output voltages lie on top of each other without deviation. Expectedly, the control error (Subfigure (b)) is negligible and according to Subfigure (d), 75 W power – respectively 25 W per module – is delivered to the load. The converter is operated at 57 kHz, which is equal to the load dependent minimal operating frequency, see Subfigure (c).

Figures 5.6 and 5.7 gives the simulation snapshots of the simulation runs with mistuned resonance capacitance. Subfigures 5.6a and 5.7a give the output voltages of the three converter modules, whereas the first two voltages apply for the nominally parametrized modules and the third voltage represents the module with negative, respectively positive, mistuned C_r. The according output voltage control error is plotted in Subfigures (b), Subfigure (c) gives the converter switching frequency f_sw and the minimal switching frequency $f_\mathrm{sw,min}$. The overall converter power, delivered to the load, is shown in Subfigure (d). The parameter variations influence on the resonance frequencies is summed up in Table 5.3.
The simulation results for $-25\,\%$ C_r deviation show that the altered modules output voltage reaches only 42.4 V under full load, which is a significant decline of $-39\,\%$ versus the nominal 70 V. The control error of the converter output voltage drops to $-13\,\%$ according to Figure 5.6b, which is a third of the module output deviation – due to three series connected converters. During the simulation, the converter operates at a stable switching frequency of 57.2 kHz, again, this represents the converters lower switching limit. With 63.8 W the load power lies $-8.9\,\%$ below the nominal load power (see Subfigures (c), (d), respectively).
With the $+25\,\%$ deviation of C_r, given in Figure 5.7, the third module's output voltage lies at 62.2 V, which is $-11\,\%$ below the nominal voltage, this yields a control error of $-3.8\,\%$. During this simulation, the converter is operated at its load point dependent

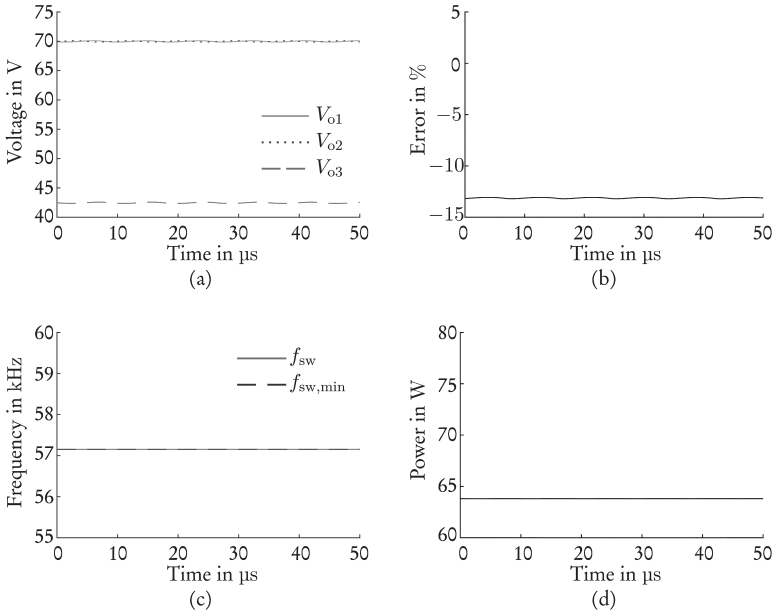


Figure 5.6.: Input-parallel, output-series converter with resonance frequency variance by resonance capacitor C_r detuning by $-25\,\%$ in the 3rd converter module.

minimal switching frequency of $57.1\,\mathrm{kHz}$. The load power is reduced to $73.2\,\mathrm{W}$, which is $2.4\,\%$ below the nominal power.

The cause of the deviation lies in the shifted resonance frequency of the altered module as given in Table 5.3. A reduction of C_r by $25\,\%$ increases the resonance frequency f_r and the lower resonance frequency f_{r1} by about $15\,\%$. With the right-shifted resonance frequency, the manipulated module is operated on the positive slope of its gain characteristics, hence to increase the module voltage, increased operating frequency is required. Due to the design, where the converter is operated on the negative slope of its gain characteristics, the voltage controller decreases f_{sw} to compensate the negative control error until either the remaining modules compensate the lagging voltage and load contribution of the mistuned module, or – like in this simulation – until the operating frequency's minimum is reached. The remaining modules' narrow gain reserve is not sufficient to compensate the lack of output voltage and load power from the manipulated module. At least not with the applied control

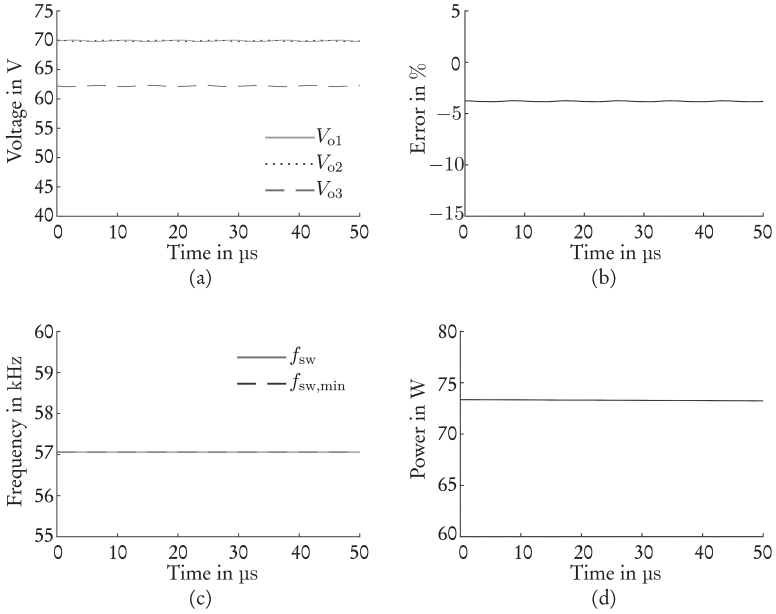


Figure 5.7.: Simulation results of resonance capacitor C_r value increased by $25\,\%$ in the 3rd module in an input-parallel, output-series converter configuration.

strategy of implementing one global controller for all modules. Further, the operation of the altered module on the positive slope of the gain characteristics lead to capacitive behavior of the resonance circuit, where zvs can-not be achieved for this module and increased losses are to be expected.
Increasing C_r by $25\,\%$ reduces f_r and f_{r1} by approx. $10\,\%$, in that case the mistuned module is still operated on its negative slope, where inductive converter behavior and zvs is given. Compared to the nominally parametrized modules, with the shifted resonance frequencies, the module is operated at a lower converter gain and hence distributes less to the overall conversion.
It is shown, that a shifted resonance frequency has a significant performance impact on module level, which is still visible on converter level but becomes less significant with growing number of modules. This effect is especially visible when the resonance frequency is increased and the affected module operates in the capacitive non-zvs region. The impact of a module with shifted resonance frequency on output voltage

Table 5.4.: Resonance frequency and normalized inductance values for the LLC-converter with $-50\,\%$ / $+100\,\%$ variation of the transformer's magnetizing inductance L_M.

	Parameter Deviation Value		
	$0\,\%$	$-50\,\%$	$+100\,\%$
f_r	$59.3\,\mathrm{kHz}$	$59.3\,\mathrm{kHz}$	$59.3\,\mathrm{kHz}$
Frequency deviation from nominal	–	$0\,\%$	$0\,\%$
f_r1	$25.5\,\mathrm{kHz}$	$33.1\,\mathrm{kHz}$	$18.9\,\mathrm{kHz}$
Frequency deviation from nominal	–	$28.8\,\%$	$-26\,\%$
L_n	4.4	2.2	8.8
Deviation from nominal	–	$-50\,\%$	$100\,\%$

and power can be further decreased by adding additional gain margin to the converter by design.

The simulation results for steady state simulation of the variation of L_M according to Table 5.2 are given in Figures 5.8 and 5.9 for the negative and the positive parameter variations respectively. The impact of the parameter variation on the modules' resonance frequencies and the normalized inductance L_n are summed up in Table 5.4. While the primary resonance frequency f_r remains untouched due to missing impact of L_M, the $50\,\%$ reduction of L_M increases f_r1 by approx. $30\,\%$ and the $100\,\%$ increase reduces f_r1 by $26\,\%$. This means, the reduced magnetizing inductance moves the second resonance frequency f_r1 closer towards the first one f_r, which results in a steeper curve set in the converters input to output characteristics. Respectively, the increased magnetizing inductance moves f_r1 further away from f_r with a less steep curve set in the result.

The modules output voltages for two modules with nominal parametrization and one with L_M reduced by $50\,\%$ are given in Subfigure 5.8a. Under full load, the converter operates close to the lower end of its operating frequency range, where the input to output gain is of significant size. In this operating situation, the manipulated converter, with reduced normalized inductance and steepest gain characteristics, contributes slightly more output voltage to the system than the other two. In the $-50\,\%$-case, it is approx. $1.25\,\mathrm{V}$ more. The system output voltage error is negligible (Figure 5.8b) and the load power is slightly above nominal power (Figure 5.8d). The converter operating frequency is above the operating point dependent operating frequency minimum (Figure 5.8c).
Simulation results for the L_M increased by $100\,\%$ are given in Figure 5.9. The results

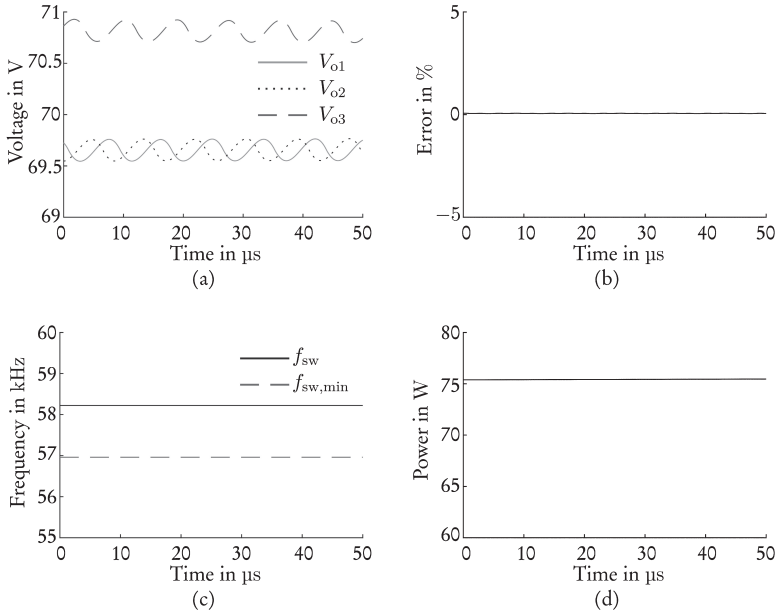


Figure 5.8.: Input parallel, output serial transformer magnetizing inductance variance. Left column: capacitor voltage of the voltage divider.

are comparable to the ones of Figure 5.8 with inverted effects. The module output voltage of the manipulated module lies at approx. $0.75\,\mathrm{V}$, slightly below the other modules' output voltage. The difference is less than in the $-50\,\%$-case simulation, due to the shallower gain characteristics in increasing frequency direction, the smaller difference is expected. Converter output voltage error and load power lie slightly below the reference values and the converter is operated at its minimum frequency.

The simulation results for the $\pm 25\,\%$ variation of the modules' series connected output capacitors C_o are given in Figures 5.10 for the negative and 5.11 for the positive variation. In this setup, the resonance circuit is not affected and hence, both resonance frequencies and the normalized inductance are equal for all three modules in all setups.

In Figure 5.10, the simulation run for the $-25\,\%$ setup shows no deviation with respect to the average module output voltage (Subfigure (a)). The converter output voltage and load power are equally distributed over all three modules. The only effect,

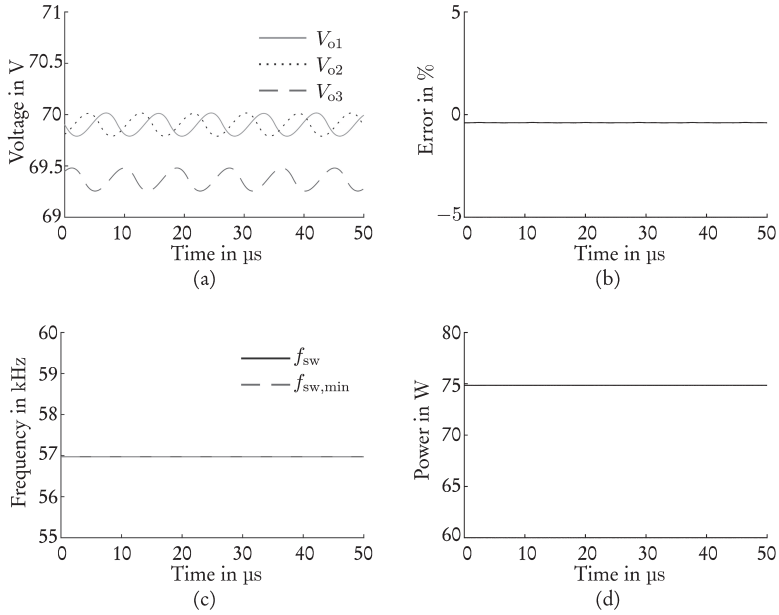


Figure 5.9.: Input parallel, output serial transformer magnetizing inductance variance.

that can be observed is a larger ripple amplitude on the converter with smaller output filter capacitor. Hence, the converter output voltage error (Subfigure (b)) is negligible and the converters output power to the load (d) equals the nominal load power. The converter is operated at its lower operating point dependent switching frequency $f_{\mathrm{sw,min}}$ (Subfigure (c)).
In comparison to the capacitance reduced by $25\,\%$, the simulation given in Figure 5.11 for the simulation case with one capacitor with increased capacitance by $25\,\%$ yields similar results. The only and expected difference is, that due to the increased capacitance, the ripple of the third module's output voltage V_3 is smaller than the ones on the first and seconds modules output voltages V_1 and V_2, respectively. Converter output voltage error, operating frequency and load power are equal to the simulation results given in Figure 5.10 and presented above.

In conclusion to the simulations in this Subchapter it can be stated, that variations with influence to the primary resonance frequency f_{r} have the most significant impact on the overall converter characteristics, as well as on the modules' operating points.

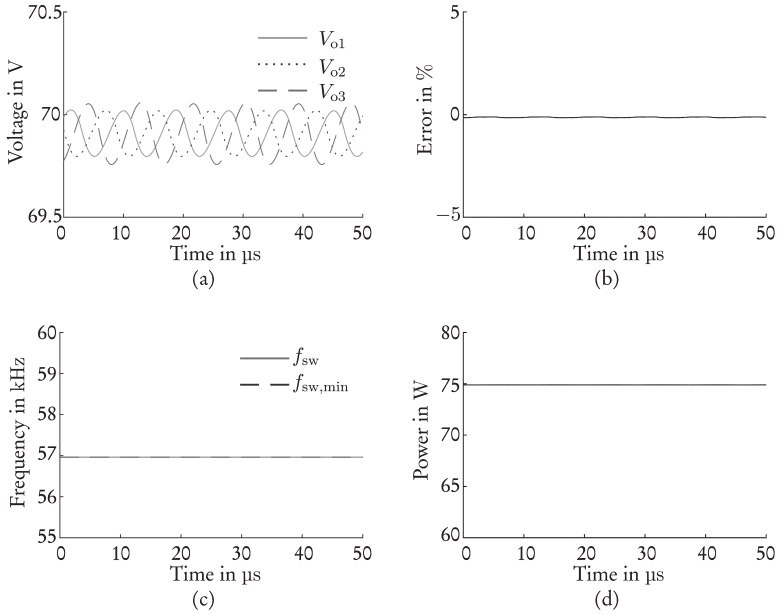


Figure 5.10.: Input parallel, output serial output capacitor variance.

This is particularly significant, if f_r is increased far enough, so that the affected modules operating point tilts over the gain characteristics maximum and is operated on the positive slope in the capacitive region. In an extreme case, this may lead to an operation, where one module transmits hardly any power. If this cannot be compensated by the remaining modules – e.g., due to a large number of modules in the system or sufficient gain reserve, the converter design goal can no longer be reached.
The impact of the variation of the normalized inductance L_n on the affected converter module is limited to the gain characteristics steepness and the maximally achievable converter gain with inverse behavior versus increasing/decreasing L_n. On modular converter level, the impact depends on whether L_n is decreased or increased. While gain characteristics steepness and maximal gain increase with decreased L_n, the converter remains capable to achieve the designed output voltage and load power, but voltage and load are no longer equally distributed between the modules. With increased L_n the operating region for high load moves below the minimum operating frequency, where the converter is blocked from operation by the voltage controller.

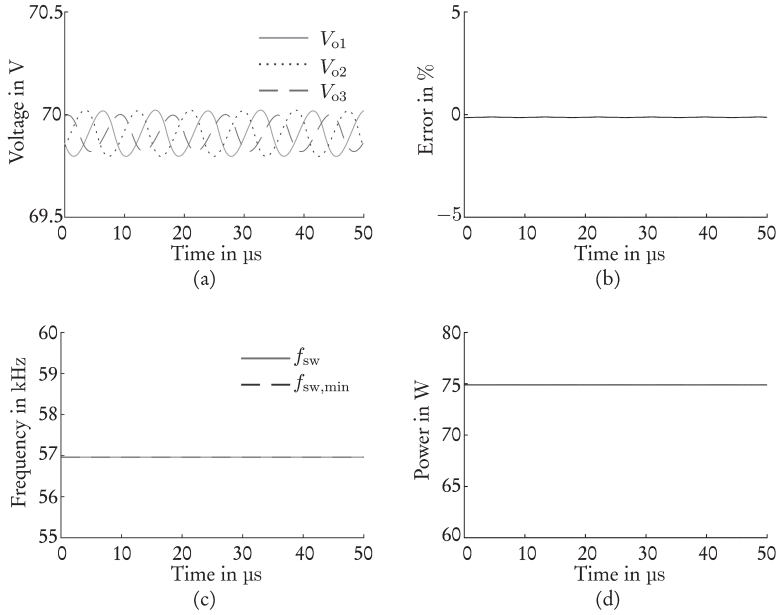


Figure 5.11.: Input parallel, output serial output capacitor variance.

Hence, at maximum power, the nominal converter output voltage and load power are not reached.
The last investigated parameter is the capacitance of the capacitive voltage divider on the modular converter's output terminals. Variation in this quantity only affects the ripple amplitude on the DC output voltage without influence on the voltage or power distribution between the converter modules.

5.3. Experimental Test Results

With the fundamental converter concept proven in simulation, a modular prototypical demonstrator of the converter is set up and integrated on a HIL test bench for experimental confirmation of the simulation results. The prototype is implemented in a scaled low voltage environment with reduced converter power. This state-of-the-art

Table 5.5.: Resonance frequency values for the LLC-converter with varied resonance frequency.

Applied Loads	*Applied Frequency Range*	
	min	*max*
2200 Ω	35 kHz	70 kHz
1100 Ω	32 kHz	70 kHz
733 Ω	30 kHz	70 kHz
550 Ω	30 kHz	70 kHz
440 Ω	32 kHz	70 kHz
366 Ω	35 kHz	70 kHz

method for evaluation of power electronic concepts simplifies the prototype handling in the laboratory, while the general validity of the experimental results remain intact. The demonstrator prototype design and parametrization are documented in Appendix B.2 and the test setup in Appendix B.3. The experimental evaluation is initiated by comparison of characteristic converter features in simulation versus measurements. The goal of these experiments is to gain evidence over the simulation results accuracy versus the test setup on one side and gaining a first proof of function for the prototype on the other side.
Subsequently, the controller performance is experimentally evaluated on a single module setup and on a modular setup with two modules in parallel-input serial-output configuration. The control and data acquisition software is executed on a real time computer for rapid prototyping purpose, which is part of the HIL environment. The controller software on the real time computer is auto-coded and build from the controller simulation models used for the simulative evaluations in Section 5.2.

5.3.1. Model and Prototype Validation

First of all, converter model and prototype are validated by comparing the converter gain characteristics of a single converter module and secondly by charging a completely discharged output capacitor with constant converter switching frequency f_{sw}. The results from simulation and prototype measurements are compared to each other and the results are discussed. Since the simulation models are validated on module basis against theory from literature in Section 5.1, confidence exists that in principle, the converter simulation model represents an LLC resonance switching DC/DC converter with all its characteristics. The introducing paragraph to this Chapter states

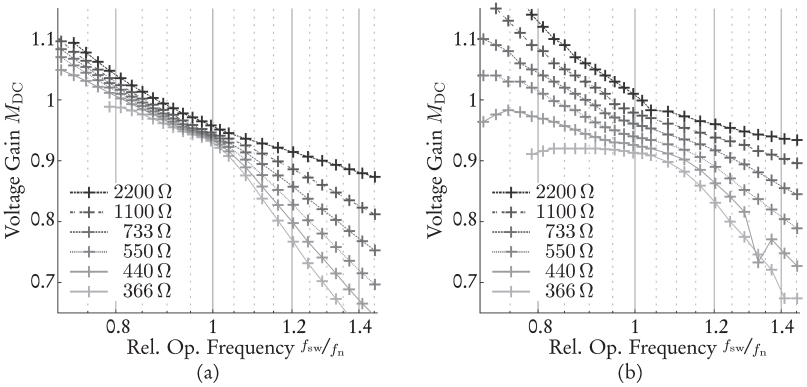


Figure 5.12.: Converter DC output voltage at given operating voltage with load according to Table 5.5 from simulation and measurement data in Subfigure (a) and (b), respectively.

that for this project, the applied simulation method delivers sufficiently accurate results for simulation of power electronic circuits. In this context, sufficiently accurate means that the converters input to output characteristic gain curves in simulation and experiment are in comparable relation within the converter's frequency and load operating range. For a minimum, the principal gain characteristics of simulation and experiment shall represent similar shapes. Gain deviations can be quantized and considered in the evaluation. Knowing that the simulation model represents an LLC resonance converter the prototype operates as desired, if simulated and measured gain characteristics sufficiently match.

The simulated and measured gain characteristic curves are generated by applying a series of fixed, resistive loads to a single module converter and operating (simulatively or experimentally respectively) the converter with a series of fixed operating frequencies according to Table 5.5. In the converters output steady state, the voltage gain is captured and with all operating points, the gain characteristics, as given in Figure 5.12 are generated. The simulated gain characteristics in Subfigure (a) show a sharp bend shortly to the right to of the converter's resonance frequency and beneath this bend, the converter gain decreases are represented by straight lines for all load cases – this is a deviation from theory, which should not be of any specific significance. At resonance frequency, theory proposes unity gain for all loads, but the simulation does not reach unity for this frequency and the gain drops further with increasing load. The observed

deviation of the load gain can be explained by the simplifications, generally made in literature, when modeling an LLC converter for gain characteristics computation: The common FHA method neglects the voltage drop within the converter's inverter and rectifier and resistive loses in the complete electrical circuits, this leads to a noticeable voltage drop plus an additional current-dependent voltage drop when simulated from a physical model such as this. The converter gain characteristics for the same converter with equal parametrization but from prototype measurements is given in Subfigure (b), it shows the characteristic gain curves of an LLC resonance converter with the above discussed deviation regarding the converter gain at resonance frequency. At operating frequency $f_{\mathrm{sw}} = 1.33 \cdot f_{\mathrm{r}}$, the measuring point of the characteristic curve for $R_{\mathrm{L}} = 1100\,\Omega$ lies well below the value expected from its directly adjacent measurement points. Obviously, this traces back to a measurement fault and hence is ignored in the analysis. Compared to the simulated gain characteristics, the prototype shows few significant deviations. At resonance frequency, unity gain is reached for light load, while for full load, the achieved voltage gain lies $-2\,\%$ below the simulated voltage gain. For light load, the measured gain lies above the simulated gain curve for all frequencies and the curve flattens out with increasing operating frequency f_{sw}, for decreasing f_{sw}, this might become significant, especially during start-up, where small gains are to be achieved under idle condition. For the high load characteristics, the measured gain lies above the simulated gain in high operating frequency conditions. At resonance frequency, the measured gain has already dropped below the simulated gain (see above). Moving to the graphs left, the gain hardly increases anymore so that the deviation between simulation and experiment is the most significant for high load and low f_{sw}. With this observation, it shall be expected, that the converter will not achieve the full nominal output voltage under full load.

For the second validation of the converter simulation model versus the prototype, the step response of the capacitor voltage versus the converter switching frequency f_{sw} is evaluated. For the data acquisition, the output capacitor charge voltage curve in response to a step function excitation of f_{sw} under equal conditions in the simulation and with the prototype. In the initial state, the output capacitor voltage is equal $0\,\mathrm{V}$ and a load resistor of $R_{\mathrm{L}} = 1100\,\Omega$ is applied. The converter is then actuated under constant switching frequency $f_{\mathrm{sw}} = 58\,\mathrm{kHz}$ without feedback control while the capacitor charges. In the prototype measurement, the capacitor voltage is recorded with a digital memory oscilloscope. The oscilloscopes trigger is set to $V_{\mathrm{o}} = 10\,\mathrm{V}$, hence in the recorded date, the first few ms are missing, which results in a mismatch of the time sequence between the measured and the simulation voltage curve of $\Delta t = 220\,\mathrm{ms}$. This mismatch is compensated by a negative time-shift by Δt of the simulated data.

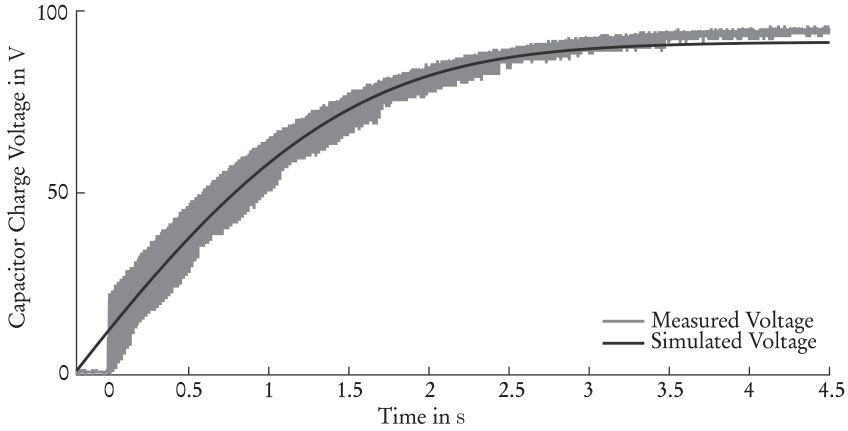


Figure 5.13.: Comparison of the measured versus the simulated output capacitor charge voltage.

Table 5.6.: Electronic load setting and resulting theoretical converter load at nominal output voltage $V_\mathrm{o} = 70\,\mathrm{V}$

Load Setting	*Load Resistance*	*Theoretical Load Power*
Full Load	$175\,\Omega$	28 W
Half Load	$315\,\Omega$	16 W

The simulation and measurement results of the output capacitor charging during the step response experiment with step to switching frequency $f_\mathrm{sw} = 58\,\mathrm{kHz}$ is presented in Fig. 5.13. The simulated curve form and rate of the voltage rise reasonably matches the measured voltage. Both curves describe the dynamic behavior, that is typical for PT-1 systems, with instantaneously rising voltage and asymptotical approach of the final value. The measured final value is reached after 4 – 4.5 s and lies at approx. $V_\mathrm{o,inf} \approx 94.5\,\mathrm{V}$, which is $103.5\,\%$ of the simulated value $V_\mathrm{o,inf} = 91.33\,\mathrm{V}$.

5.3.2. Single Model Control Performance

This section documents the controller performance evaluation on one single prototype converter module in the HIL test setup. Therefore, the controller software, auto generated from the control law in Subsections 4.2.2 – 4.2.5, is transferred to the test

setup from Appendix B.3. In the first step, the converter start-up routine is executed and recorded with sample rate $T_\mathrm{s} = 10\,\mathrm{ms}$ on the HIL. According to the configuration parameters in Table 5.6, the electronic load on the HIL is configured to full converter load on one channel and half load on the second. The benchmark test from Section 4.2.6 is then executed by manual activation of the load and manual switching between both channels, hence the time periods in the recorded dataset do not match the definitions of the benchmark test, which has no effect on the measurement quality.

Each subfigure of Figure 5.14 shows two plots, the left plots show the results of the experimental converter startup and the right ones give the measurement results for the benchmark test. Note that the ordinate scaling holds true for both plots and is only given on the figure's outside for better readability. The time scale for the startup routine and the benchmark test is configured independent from each other and both start at zero. Subfigure (a) shows the converter input voltage, measured directly on the converter prototype. The converter output voltage and its reference trajectory are plotted against the left ordinate of Subfigure (b), in the same subfigure, the converter load current is plotted against the right ordinate. In the figure's startup part, the current is too low to be visible due to scaling optimized for the benchmark test. The converter operating frequency f_sw and the load point dependent minimum operating frequency to the left ordinate and the converters output voltage control error to the right ordinate are plotted in Subfigure (c). Subfigure (d) depicts the converter load during startup and the benchmark test.

From simulation, the converter output voltage V_o is expected to initially rise to $40\,\mathrm{V}$ but in Subfigure (b) it gets as high as $V_\mathrm{o} = 50\,\mathrm{V}$. Once, the reference trajectory reaches $50\,\mathrm{V}$, the output voltage is picked up, the feedback controller activation in this time instance is noticeable with a slight dip of the actuation frequency (Subfigure (c)). Once picked up, V_o follows the reference with slight oscillation around it within an approx. $\pm 5\,\%$-error band. The voltage overshoot of $\Delta V_\mathrm{p} = 0.2\,\mathrm{V}$ at the final converter voltage is negligible. The output voltage, initially too high, can be explained partially with the results from the gain map comparison in Section 5.3.1. Under light load and high operating frequencies, the prototype yields higher converter gain than the simulated model, for $f_\mathrm{sw} = 70\,\mathrm{kHz}$ – which is the highest operating frequency in the gain maps – the prototype lies $7\,\%$ above the simulation, with diverging trend lines. Secondly, the simulated output voltage quickly rises to $40\,\mathrm{V}$, but without controller interference, V_o slowly continues to rise, hence the stated $40\,\mathrm{V}$ is not the steady state value. With these two effects, the deviation of $25\,\%$ at $f_\mathrm{sw} = 120\,\mathrm{kHz}$ is sufficiently justified.
In the plots benchmark section, the initial load jump from $P_\mathrm{Load} = 0\,\mathrm{W}$ to $P_\mathrm{Load} = P_\mathrm{nom}$ converter load leads to a significant voltage drop as low as $V_\mathrm{o} = 45\,\mathrm{V}$ and settles at $V_\mathrm{o} = 62.7\,\mathrm{V}$ approx. $70\,\mathrm{ms}$ after the minimum and $90\,\mathrm{ms}$ after the beginning of the

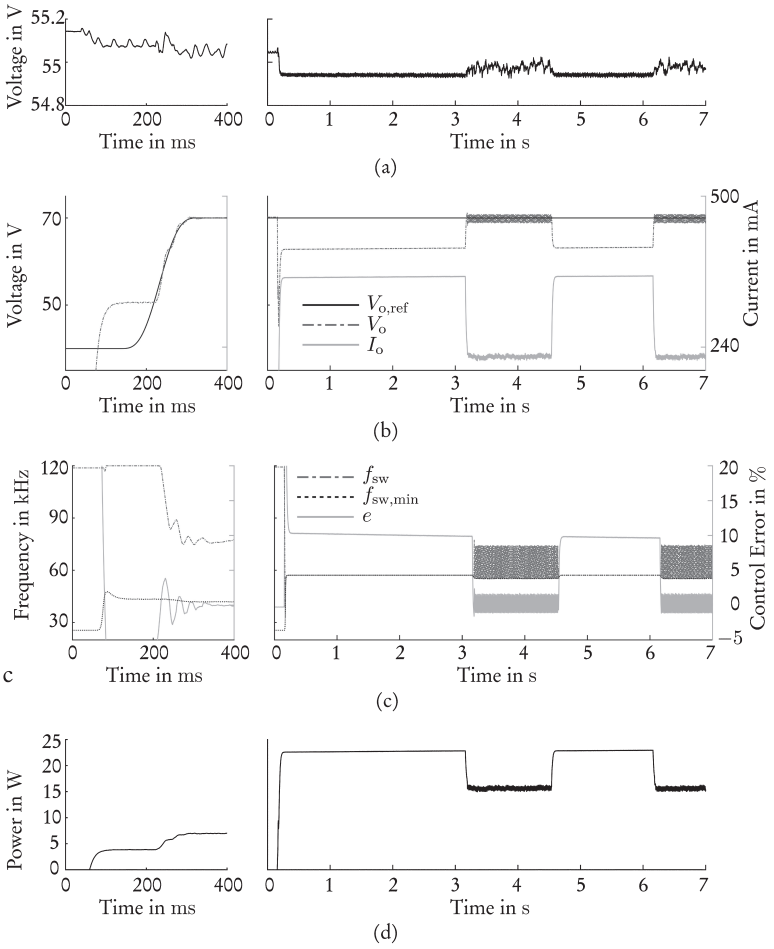


Figure 5.14.: Results from experiment with one scaled prototype converter module: Subfigure (a): Converter input voltage. Subfigure (b): Output voltage reference vs. actual value on left and output current on right ordinate. Subfigure (c): Operating frequency, minimum frequency (left ordinate) and control error (right ordinate). Subfigure (d): DC output power.

load step. Over the full load phase duration of $3\,\mathrm{s}$, the output voltage rises by $0.2\,\mathrm{V}$, this corresponds to a control error of approx. $-10\,\%$. The input voltage sag during full load accounts for negligible $0.06\,\mathrm{V}$. The converter load reaches $P_{\mathrm{Load}} = 22.8\,\mathrm{W}$ during full load, where it is set to reach $25\,\mathrm{W}$. At the same time, the converter is operated at its load dependent minimum operating frequency, hence $22.8\,\mathrm{W}$ is the maximum load, the prototype can achieve. In the transition to half load the converter output voltage returns without noticeable overshoot to its nominal output voltage. The subsequent half load operation is executed at nominal output voltage, the load oscillates in the range $P_{\mathrm{Load}} = [15, 16.3]\,\mathrm{W}$, as the operating frequency does in parallel. The load jumps from half to full and back to half load. It now shows additional noticeable behavior.
The significant voltage drop during the transition from idle to full load deviates from the expected behavior with respect to the according simulation result in Subsection 5.2.2 and hence requires explanation. The most significant setup difference to the simulation is the way, the converter load is emulated; in the HIL setup an electronic load in resistive mode is applied as load. For the benchmark test, the activation of the electronic load represents the benchmark's initial load jump from $P_{\mathrm{Load}} = 0\,\mathrm{W}$ to $P_{\mathrm{Load}} = P_{\mathrm{nom}}$ converter load. This load jump, executed by the electronic load turn-on is steeper than the one defined in the benchmark and hence steeper than the one simulated. With the electronic load, the in-detail functionality is not known, but the voltage curve during load activation is characteristic for immediate charging of a discharged input-capacitor. Due to these characteristics, it is assumed, that the electronic load features an input capacitor, which is instantaneously connected to the converter output during activation of the load.
The voltage error in the steady state under full converter load matches the deviation between maximal voltage gain under full load between simulation and experiment in Figure 5.12. This effect can be explained by insufficient prototype design, here the transformer as non-out-of-stock component is likely the candidate for the problem's root. With magnetic coupling below the desired grade or the core going into saturation, the power transfer might be limited, where it is not expected. It is further noticeable, that the converter operates on its lower operating frequency limit, this limit is computed from theoretical parametrization – although with parameter correction from testing – hence, it could limit the converter performance if it is seated right of the load-dependent gain peak by preventing the converter from exploiting its complete capability. On the other hand, a conservative choice of the frequency limit safely prevents the converter from operating in its capacitive region, where losses rise due to loss of zvs.

The evaluation of the single module LLC converter prototype in an HIL setup revealed few shortcomings regarding the voltage stabilization, especially under high load. This leads to a behavior deviating from the simulated converter behavior within

Table 5.7.: Electronic load setting and resulting theoretical converter load at nominal output voltage $V_o = 140\,\mathrm{V}$

Load Setting	*Load Configuration*	*Theoretical Load Power*	*Actual Load Resistance*	*Actual Load Power*
Full Load	$392\,\Omega$	$50\,\mathrm{W}$	$392\,\Omega$	$42.4\,\mathrm{W}$
Half Load	$784\,\Omega$	$25\,\mathrm{W}$	$742\,\Omega$	$32.5\,\mathrm{W}$

the startup routine, where the initial voltage rise is higher than expected, this behavior is acceptable without limitation. Under full load, the output voltage and desired load power are not reached, which limits the significance of this experiment. Nevertheless, in an overall perspective it is still visible, that the combination of converter architecture and controller software are capable to fulfill the desired functionality – with improved prototyping design. The discussed shortcomings are taken into account for the following experimental evaluation of the modular converter prototype.

5.3.3. Modular DC/DC Converter under Experimental Testing

For the experimental evaluation of the modular converter, two converter modules are set up in input-parallel, output-series connection on the HIL as documented in Appendix B.3. The voltage control is implemented according to the global control concept for modular DC/DC converters from Subsection 4.3.2. Again, the software code is auto generated and uploaded to the HIL real time computer in the same way, as for the single module experiment. Like in the forgoing sections, the startup routine and the benchmark test are applied for evaluation – with adapted load scaling for the modular converter.

Figure 5.15 gives the measurements from experiment, that document the converter startup routine in the left subgraph and the benchmark test for the modular converter setup in the right subgraph. The time scaling and offset is individually tuned for the startup and the benchmark test. The converter DC input voltage in Subfigure (a) remains well within $\pm 0.5\,\mathrm{V}$ of the nominal input voltage of $V_{\mathrm{in}} = 55\,\mathrm{V}$ during the complete experiment. In Subfigure (b) the converter output voltage reference and measured output voltage is plotted versus the left und the converter output current versus the right ordinate. In the startup plot, the converter is activated at $t = 4\,\mathrm{ms}$, with $64\,\mathrm{ms}$ delay, the output voltage reaches the initial reference voltage. From there, it follows the rising soft-start reference trajectory in an oscillating waveform to the final converter output voltage without overshoot. In this section, the electronic

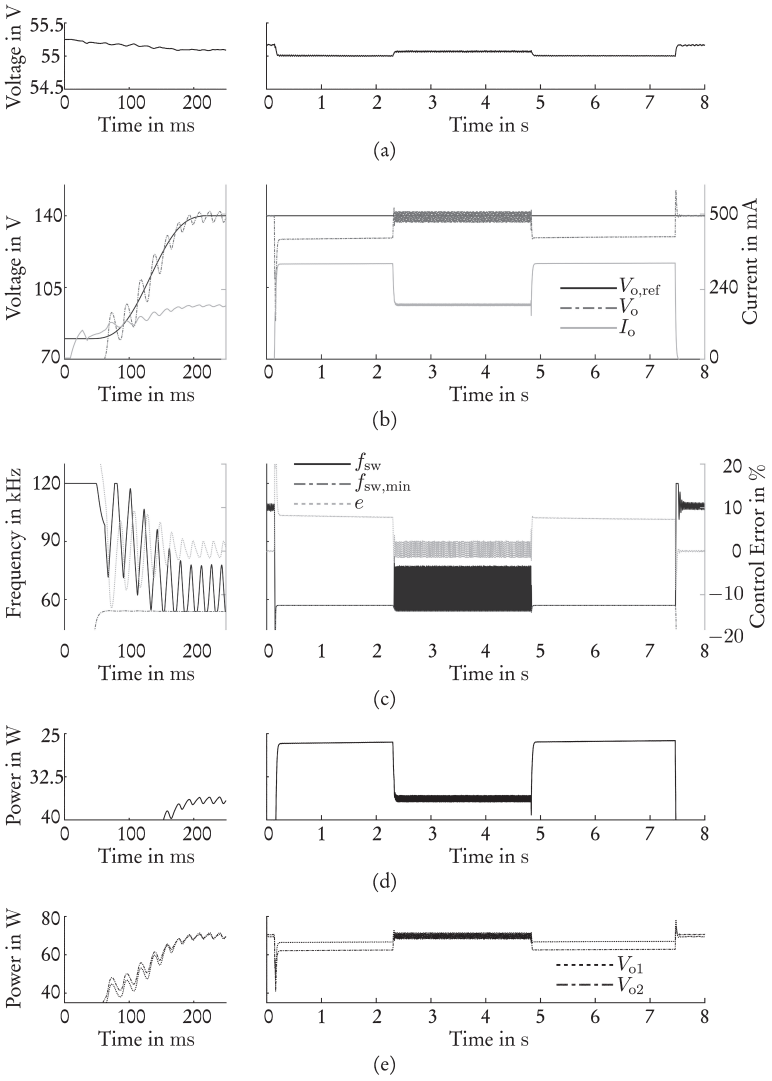


Figure 5.15.: Results from experiment with a set of two scaled prototype, which are input-parallel, output-serial connected. Subfigure (c) gives the semiconductor switching frequency, (a) the converter DC input voltage, (b) DC output voltage reference and actual value on the left and output current on the right scale, (d) gives the DC output power and (e) the module output voltages.

load is already set to half load to avoid the initial voltage drop, for details refer to the single module experiment in Section 5.3.2. In the Figures right graphs, the first load step to full load is initiated approx. at $t = 0.142\,\mathrm{s}$, after this step the output voltage immediately drops to approx. $V_\mathrm{o} = 89\,\mathrm{V}$ and rises back to approx. $129\,\mathrm{V}$, the complete voltage dip takes about $90\,\mathrm{ms}$. With the return of the output voltage from the dip, the output current rises to $327\,\mathrm{mA}$ without overshoot. In the following full load phase, the converter is operated at its load-dependent minimum frequency, wherefore the converter voltage cannot further rise towards its nominal value. During full load phase, the output current slightly rises to $I_\mathrm{o} = 330\,\mathrm{mA}$, note that the load equivalent resistance for full load in Table 5.7 is computed with this value. The load power (Subfigure (d)) in the full load phase reaches $P_\mathrm{Load} = 42.5\,\mathrm{W}$ (intended load: $50\,\mathrm{W}$). The delta from actual to intended load results from the converter operation at minimum operating frequency, leading to reduced output voltage during this part of the experiment – equal to the single module experiment. In the subsequent transition from full to half load, the converter output returns back to nominal voltage with a slight overshoot of $\Delta V_\mathrm{p} = 3.8\,\mathrm{V}$. With $P_\mathrm{Load} = 32.5\,\mathrm{W}$ the half load output power lies $30\,\%$ above the desired $25\,\mathrm{W}$. This is traced back to the electronic load: During the experiment it was multiply observed, that the load provides a lower load resistance than configured on the devices interface. Further, the half load phase and transition to full load behaves comparable to the single module experiment with increased but stable voltage ripples. In the final turn-off transition, where the electronic load is set to standby under full load, a voltage peak of $V_\mathrm{o} = 152.6\,\mathrm{V}$ is observed, subsequently, the output voltage is stabilized at nominal voltage. The module output voltage is depicted in Subfigure 5.15e. It shows, that during startup and light load, the output voltages of both modules lie well above each other, while under full load, one module contributes higher voltage to the overall converters output voltage than the other. The delta between both accounts for $4.3\,\mathrm{V}$ respectively approx. $7\,\%$.

The experiments in this section prove the concept of the utilization of modular LLC converters to generate high DC voltage. It shows, that the voltage and power is equally distributed between the involved converter modules – little deviations included. The applied voltage controller deliberately works without individual error compensation per module to realize a concept where all modules are actuated with the same inverter frequency and symmetrical phase delay between the modules to achieve good DC filtering characteristics. The voltage controller smoothly steers the output voltage alongside the startup trajectory to the aimed converter output voltage. The voltage stabilization during the benchmark test is acceptable, the observed deviation to the ideal behavior, or to the simulation results respectively, is explained by poor prototype design.

6. Conclusion and Future Work

In this work, a concept for a high voltage DC/DC converter, where the HV terminal voltage is distributed over a number of converter modules was presented. By the distribution of the voltage over the modules, the module terminal voltage can be kept comparably small, which allows the usage of technologies, that are only available for moderate voltage, as fast switching semiconductor switches. The voltage distribution is utilized either on the input- or output-terminal side, wherever high voltage is processed. If one side of the converter operates in low voltage, the terminals of the single modules are connected in parallel, then all modules experience the full terminal voltage and the terminal current is distributed over the modules. For the single modules, an LLC resonance converter hardware architecture with full bridge inverter and rectifier was proposed. This converter type features low current semiconductor turnoff (quasi zcs) for the inverter and zvs turn-on for the rectifier diodes, which increases the converter efficiency and is an enabler for fast switching. Fast switching is a key property for high volumetric and gravitational power density. The converter input side is galvanically isolated from the output by a transformer in the power path. For the auxiliary circuits, a concept for galvanic isolation was given to achieve full input to output to environment isolation for safety and protective means.
For simulation purposes, the system was modeled with a computer numeric software package, extended by a physical modeling toolbox. Comparison between the expected waveforms in the converter's resonance circuit and the rectifier showed few deviations, that could be explained by model characteristics and the simulation model could be validated against theory on module level. With a scaled prototypical implementation available, the simulation module was validated by comparing the converter gain characteristics from simulation and from prototype measurements. Here, especially in the extreme operating regions, deviations between the models input to output gain characteristics versus the prototype measurements were observed and their significance was explained. In a second test, a constant inverter switching frequency f_{sw} was applied to an LLC converter with fully discharged bulk capacitor and the capacitor charging curve was recorded in simulation and in the prototype experiment. Both plots lie well above each other, indicating good conformity of the dynamic behavior of model and prototype.
For the combination of modules to an HV converter, the converter behavior under

component tolerances was evaluated by simulation. Analysis showed, that the most significant impact to the input to output power transmission is caused by the components, which are directly part of the resonance circuit, due to their influence on the resonance frequency. Here, zcs in the inverter semiconductors can be lost and in an extreme case, power transfer cannot be achieved any more. To meet those challenges, it was found favorable to apply a combination of counteractions, which are adding sufficient safety margins while engineering the converter and utilization of a large number of modules.

The HV converter was set into context of two possible applications, which are

- Offshore wind farms:
  Direct DC connection to HVDC transmission lines without AC coupling.

- Tethered mobile machines:
  Energy supply with DC transmission lines to enable higher machine power, respectively longer transmission lines.

On current wind farm topologies, each turbine features an inverter, that feeds the electrical energy to the wind farms low voltage AC grid. In one central transmission knot, the energy is either transformed to HVAC and directly transferred to shore or the HVAC is rectified and transmitted by HVDC. For the energy transmission to shore, the future clearly lies in HVDC transmission. Therefore, it was proposed to apply the converter concept, presented within this work for a wind farm architecture, comparable to [HBM+13, MP15].
For the tethered mobile machines, the converter was identified as a key component of the HVDC tethering system, that can lead to higher machine power and – over longer transmission lines – to a lager radius of action for the machine. This makes the new tethering system with high power density a possible enabler to push tethered mobile machines into additional markets, where high power and large action radii are required, as for agricultural machinery. Further, an energy management, where no communication is required on the tethering line, was proposed for such an energy supply system. The machine side HV converter controls the energy flow to the machine, according to the machines demand. The stationary side converter, that generates the high voltage for energy transmission, stabilizes the line voltage from measurement data and needs no commanding signals from the machine.

For the converter output voltage control, the LLC converter was theoretically analyzed under the assumption, that the converter input rectifier displays a nearly ideal, variable frequency AC voltage source with rectangular waveform. For the models output, the converter DC output voltage was chosen. The analysis yielded a switched linear system of grade 5 with three switching states, where the switching is initiated

by the sign change of the rectifiers AC input current. Global, asymptotic Lyapunov stability was proven by successful computation of a CQLF.
The voltage stabilization concept was structured in such a way that a control concept was developed for the LLC converter module and subsequently was set in a superordinate context for the HV converter. The module control relies on a model-based pilot control by static gain characteristics, that were implemented in a lockup table for efficient online computation and a parallel PID feedback controller to compensate control errors from dynamic system behavior and model inaccuracies. For the control reference generator, a trajectory, that starts with the minimal voltage, the converter can provide within the actuator operating range ($f_{\mathrm{sw,min}} - f_{\mathrm{sw,max}}$), was computed a priori for converter soft start. The converter output voltage is capable to exactly follow the reference trajectory, this limits the inrush current to the bulk capacitor.
Simulative and prototype evaluation of the LLC converter module controller were performed for the startup behavior and the voltage control under power delivery. The soft-start experiments showed initial voltage deviation, that was compensated before the final voltage was reached. The prototype's deviation was greater since the initial voltage rise was larger than expected. Nevertheless, the converter was steered to the final output voltage with negligible voltage overshoot. During the soft startup the output current never exceeded $400\,\mathrm{mA}$, which is well below the converters nominal current of approx. $600\,\mathrm{mA}$. With these experiments, the soft-start goals of reducing converter stress by avoidance of output voltage overshoot and large capacitor inrush current was proven. For the control performance during power delivery, a benchmark test was defined within this project, with the goal to represent full-, half load and idle state, as well as a variety of load steps to receive a good representation of the converter load spectrum. While simulation showed good controller performance without significant control error and overshoots, the prototype experiments did not reach the full load power and reacted to (positive) load changes with unexpected voltage drops. Those deviations within the prototype experiments were justified by limitations of the used prototype and likely by the electronic load's behavior, applied in the HIL setup. The LLC converter module experiments were closed with the conclusion, that the converter control operates sufficiently well to guaranty safe startup and stable output voltage control operation.

To control the output voltage of a high voltage DC/DC converter, consisting of a number of LLC converter modules, two fundamental strategies were lined out and compared against each other. In the first concept, each converter module features its own control loop. The module output voltage is measured and directly fed back to the module's voltage controller. Within the system, one reference for all modules is generated and is supplied to each module. The control variable is independently computed for each module and guarantees best control performance on module level. Due to the variable inverter switching frequency, every converter module operates at

its own frequency, consequently output ripple reduction by phase shifted operation is not feasible for this control setup. In the consequence, voltage ripples are irregular in amplitude and frequency, with rather low frequency and larger bulk capacitors are needed for good filtering effect. Alternatively, and favored, one global controller was proposed which computes one control value for all converter modules. While all modules are operated at equal operating frequency, the inverters can be operated with evenly distributed phase shift, which increases the output ripple frequency and reduces the necessary bulk capacitance for good filtering effect. This control concept does not compensate each modules unique deviations from the design quantities but computes an average compensation, so some modules will contribute more, and some modules less output voltage/power. With respect to this circumstance, it was emphasized, that deviation of the modules from the nominal operating point must be considered during the design process and respective margins must be added to the operating area.
The global controller concept was successfully evaluated by simulation and prototypical experiment in an equal manner as the controller for the LLC converter module. Both, startup and benchmark experiments showed good performance in simulation and acceptable deviations during the HIL test. During startup, voltage overshoots and high bulk capacitor inrush currents were reliably avoided. As during the module measurements, the modular converters initial voltage lay above the theocratically expected value, but the impact to the critical parameters during startup – capacitor inrush current and voltage overshoot – were without significance. During the benchmark test, the shortcomings, that were already documented for the module-level HIL test were again observed. Apart from this, the system operated as expected, hence the fundamental converter concept and the accompanying control law are proven in functionality.

Future work with respect to this publication shall focus on continuing the theoretical system analysis in the switched linear time domain. Therefore, an in-depth analysis of the systems observability and controllability shall be performed. This may be based on the work by Egerstedt and Babaali [EB05], who published a method to investigate a discrete-time switched linear system on observability and controllability. Since the system within this publication is modeled in the continuous time domain, it needs to be transformed to the discrete-time domain for working with the algorithms from the given article. Further literature on this subject was published, among others, by Trenn et all. in [TT10] for observability and Küsters et al. [KRT15] for controllability. Confidence, regarding observability and controllability is necessary, if control laws such as state controllers shall be evaluated with this system. Nevertheless, computation of those two characteristics appears to be rather challenging in praxis.
Continuing on the theoretical side, the switched linear state space model, given for the converter circuit shall be extended over the closed control loop. Therefore, the control low must be modeled by (switched-linear) differential equations, yielding the

control variable f_{sw} as output. The mathematical description of the relation from the control variable to the actual converter input voltage is also still pending and hence needs to be modeled. The later will lead to an additional switching variable and an interesting problem, of how the switching is updated by a varying switching frequency. With the received switched linear state model of the converter system in closed control loop mode, the converter under voltage control can by analyzed regarding stability with the CQLF method, applied within this work. Furthermore, with this preliminary work, a good foundation regarding robustness analysis of the controlled converter system is given.

On the applicational side, future work shall concentrate on continuing prototypical experiments towards a larger voltage and power scale. Thereby, confidence regarding the systems functioning in the high voltage domain shall be gained. In this process, the prototypical control computer could be replaced by an embedded system that is suitable for operation on a mobile machine to prove the controller is operable on this target application, where computing resources are notoriously limited.

A. Modeling Details and Derivations

A.1. Branch and Junction Equations for a Converter Module

In this Appendix, background information according the mathematical model in Section 4.1.2 are given. Therefore, the complimentary tree from Figure A.1 is derived from the converter model in Figure 4.1b and the following set of branch and junction equations

$$v_1 = v_{\mathrm{Cr}} + v_{\mathrm{Lr}} + v_{\mathrm{R1}} + v_{\mathrm{L1}} + v_{\mathrm{M}}, \tag{A.1}$$

$$v_{\mathrm{Fe}} = v_{\mathrm{M}}, \tag{A.2}$$

$$v_{\mathrm{M}} = n v_{\mathrm{L2}} + n v_{\mathrm{R2}} + n \operatorname{sgn}(i_2) V_{\mathrm{o}}, \tag{A.3}$$

$$V_{\mathrm{o}} = V_{\mathrm{Co}}, \tag{A.4}$$

$$i_{\mathrm{Fe}} = i_1 - i_{\mathrm{M}} - \frac{1}{n} i_2, \tag{A.5}$$

$$i_2 \operatorname{sgn}(i_2) = i_{\mathrm{Co}} + I_{\mathrm{o}}. \tag{A.6}$$

is obtained.

A.2. Stability of Switched Linear Systems by Lyapunov's Direct Method

In this appendix, in detail information regarding the numeric computation of a positive definite symmetric matrix $\boldsymbol{P}$ is documented. If a matrix $\boldsymbol{P}$ can be found, a CQLF is gained for the converter switched linear system and stability is proven. The numeric investigation is run on the external *Matlab* toolbox *YALMIP*. This toolbox is multiplicately applied on equation (2.47) ($\boldsymbol{A}_\sigma^T \boldsymbol{P} + \boldsymbol{P} \boldsymbol{A}_\sigma < 0$) with all system state matrices $\sigma \in \{-1, 0, 1\}$ of the system at hand in the attempt to find a common solution for $\boldsymbol{P}$. For the actual computation, *YALMIP* can operate with external

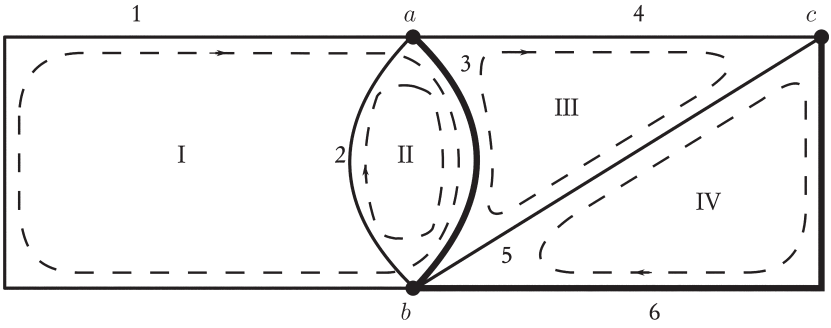


Figure A.1.: Complimentary tree of a converter module

solvers, for this project, *Sedumi* is utilized. This experiment is executed twice, once with the systems direct state matrices and once with a set of preconditioned state matrices to gain greater distance from zero for a more qualified statement.

For the CQLF solution for the systems state matrices without preconditioning, the computer numeric toolbox yields the symmetric matrix

$$\boldsymbol{P} = \begin{pmatrix} 3.11 \cdot 10^{-17} & 2.83 \cdot 10^{-18} & -5.19 \cdot 10^{-18} & -1.73 \cdot 10^{-18} & 1.71 \cdot 10^{-22} \\ 2.83 \cdot 10^{-18} & 1.19 \cdot 10^{-12} & -1.91 \cdot 10^{-13} & -2.68 \cdot 10^{-13} & 2.95 \cdot 10^{-19} \\ -5.19 \cdot 10^{-18} & -1.91 \cdot 10^{-13} & 5.29 \cdot 10^{-12} & 2.67 \cdot 10^{-13} & -2.82 \cdot 10^{-19} \\ -1.73 \cdot 10^{-18} & -2.67 \cdot 10^{-13} & 2.67 \cdot 10^{-13} & 4.20 \cdot 10^{-13} & -3.94 \cdot 10^{-19} \\ 1.70 \cdot 10^{-22} & 2.95 \cdot 10^{-19} & -2.82 \cdot 10^{-19} & -3.94 \cdot 10^{-19} & 4.60 \cdot 10^{-15} \end{pmatrix}, \tag{A.7}$$

with its sub-determinants

$$\det \boldsymbol{P_1} = 3.111 \cdot 10^{-17} \tag{A.8}$$
$$\det \boldsymbol{P_2} = 3.6995 \cdot 10^{-29} \tag{A.9}$$
$$\det \boldsymbol{P_3} = 1.9476 \cdot 10^{-40} \tag{A.10}$$
$$\det \boldsymbol{P_4} = 6.8263 \cdot 10^{-53} \tag{A.11}$$
$$\det \boldsymbol{P_5} = 3.144 \cdot 10^{-67}. \tag{A.12}$$

Hence, $\boldsymbol{P}$ is positive definite symmetric, which yields a globally asymptotically stable behavior for the LLC converters linear switched system. The smallest sub-determinant

is $\det \boldsymbol{P_5} = 3.144 \cdot 10^{-67}$, which is small but acceptable for computation on a $46\,\mathrm{bit}$ system.

In a next step, it is tested, if a more stable CQLF can be found by applying a preconditioned state matrices $\tilde{\boldsymbol{A}}_\sigma$ to the CQLF algorithm. Therefore, the switched linear system is preconditioned by the linear preconditioning method of row-wise scalar multiplication by the Euclidean norm according to [Mei15, Ch. 5.1]. Preconditioning of a linear system $\boldsymbol{Ax} = \boldsymbol{b}$ can improve its condition, although condition improvement is not guaranteed. Generally, for the preconditioning, the system transformation is

$$\boldsymbol{D}^{-1}\boldsymbol{Ax} = \boldsymbol{D}^{-1}\boldsymbol{b}, \tag{A.13}$$

with the diagonal and non-singular preconditioning matrix $\boldsymbol{D}$. [Mei15, Ch. 5] By applying the factorization $\boldsymbol{D} = \boldsymbol{T}\boldsymbol{T}^T$, the dynamic LTI systems (4.8 – 4.9) transformation is

$$\boldsymbol{T}^T\dot{\boldsymbol{x}}(t) = \left[\boldsymbol{T}^{-1}\boldsymbol{A}\boldsymbol{T}^{-T}\right]\left[\boldsymbol{T}^T\boldsymbol{x}(t)\right] + \boldsymbol{T}^T\boldsymbol{b}u(t), \tag{A.14}$$

$$y(t) = \left[\boldsymbol{c}^{\mathrm{T}}\boldsymbol{T}^{-T}\right]\left[\boldsymbol{T}^T\boldsymbol{x}(t)\right]. \tag{A.15}$$

For the equilibration, the transformation matrix $\boldsymbol{D}$ is a diagonal and non-singular matrix and it is $\boldsymbol{T}^T = \boldsymbol{T}$, hence $\boldsymbol{D}$ can be formulated by

$$\boldsymbol{D} = \mathrm{diag}(d_i) = \mathrm{diag}(t_i^2) \quad \text{for} \quad i = 1, 2, \ldots n \tag{A.16}$$

for a n-dimensional system. The optimal condition for the LTI systems (4.8 – 4.9) is achieved, if the norms of all lines of the preconditioned system $\tilde{\boldsymbol{A}} = \boldsymbol{D}\boldsymbol{A}$ are equal. If the $n \times n$ state matrix is written in line form, e.g.,

$$\boldsymbol{A} = \begin{pmatrix} \boldsymbol{l}_1 \\ \boldsymbol{l}_2 \\ \vdots \\ \boldsymbol{l}_n \end{pmatrix} \tag{A.17}$$

with

$$\boldsymbol{l}_i = \begin{pmatrix} a_{i1} & a_{i2} & \ldots & a_{in} \end{pmatrix} \quad \text{for} \quad i = 1, 2, \ldots n \tag{A.18}$$

then, the preconditioned state matrices Euclidean norm is, after some reformulation

$$\|\tilde{\boldsymbol{l}}_i\| = d_i\|\boldsymbol{l}_i\| = d_i\sqrt{\sum_{j=1}^{n} a_{ij}^2} \tag{A.19}$$

yielding

$$d_i = \frac{\|\tilde{\boldsymbol{l}}_i\|}{\sqrt{\sum_{j=1}^{n} a_{ij}^2}} \quad \forall\, i \in \{1, n\} \tag{A.20}$$

for the transformation matrices entries. In [Mei15, Ch. 5.1], $\|\tilde{\boldsymbol{l}}_i\|$ is set to unity, here we first demand

$$\|\tilde{\boldsymbol{l}}_i\| = K \quad \forall\, i \in \{1, n\} \tag{A.21}$$

and determine K in the following. Therewith, a linear system with n equations and $n+1$ unknowns is formulated. That leaves one grade of freedom. For the problem at hand, the median of the row vector norms is chosen for the remaining variable

$$K = \frac{1}{n} \sum_{i=1}^{n} \|\boldsymbol{l}_i\|. \tag{A.22}$$

Hence, for the elements of the conditioning matrix $\boldsymbol{D}$ (A.19, A.21) the preconditioning by linear equilibration yields

$$d_i = \frac{K}{\|\boldsymbol{l}_i\|} \quad \forall\, i \in \{1, n\} \tag{A.23}$$

and $\tilde{\boldsymbol{A}}_\sigma$ can be computed.

Finally, the re-computation of the CQLF with preconditioned state matrices $\tilde{\boldsymbol{A}}_\sigma$ yields

$$\boldsymbol{P} = \begin{pmatrix} 1.04 \cdot 10^{-16} & 1.15 \cdot 10^{-19} & -1.98 \cdot 10^{-16} & -5.38 \cdot 10^{-18} & -5.66 \cdot 10^{-24} \\ 1.15 \cdot 10^{-19} & 2.37 \cdot 10^{-12} & 2.21 \cdot 10^{-12} & 2.49 \cdot 10^{-13} & -8.43 \cdot 10^{-20} \\ -1.98 \cdot 10^{-16} & 2.21 \cdot 10^{-12} & 9.87 \cdot 10^{-12} & -3.90 \cdot 10^{-13} & 1.75 \cdot 10^{-19} \\ -5.38 \cdot 10^{-18} & 2.49 \cdot 10^{-13} & -3.90 \cdot 10^{-13} & 7.66 \cdot 10^{-14} & 2.00 \cdot 10^{-20} \\ -5.66 \cdot 10^{-24} & -8.43 \cdot 10^{-20} & 1.75 \cdot 10^{-19} & 2.00 \cdot 10^{-20} & 1.27 \cdot 10^{-14} \end{pmatrix} \tag{A.24}$$

$$\det \boldsymbol{P}_1 = 1.049 \cdot 10^{-16} \tag{A.25}$$

$$\det \boldsymbol{P}_2 = 2.494 \cdot 10^{-28} \tag{A.26}$$

$$\det \boldsymbol{P}_3 = 1.9465 \cdot 10^{-39} \tag{A.27}$$

$$\det \boldsymbol{P}_4 = 1.3401 \cdot 10^{-54} \tag{A.28}$$

$$\det \boldsymbol{P}_5 = 1.7114 \cdot 10^{-68} \tag{A.29}$$

Table A.1.: Conditions and boundary constraints for the computation of the converters reference voltage start up trajectory.

Start Point Time Instance	$t_0 = 0\,\mathrm{ms}$
End Point Time Instance	$t_\mathrm{e} = 200\,\mathrm{ms}$
Start Point Voltage	$V_{\mathrm{o,ref}}(t_0) = 40\,\mathrm{V}$
Derivatives in the Start Point	$\frac{\mathrm{d}^i V_{\mathrm{o,ref}}(t_0)}{\mathrm{d}t^i} = 0\,\mathrm{V/s}^i \quad \forall\, i \in \{1, r=3\}$
End Point Voltage	$V_{\mathrm{o,ref}}(t_\mathrm{e}) = 70\,\mathrm{V}$
Derivatives in the End Point	$\frac{\mathrm{d}^i V_{\mathrm{o,ref}}(t_\mathrm{e})}{\mathrm{d}t^i} = 0\,\mathrm{V/s}^i \quad \forall\, i \in \{1, r=3\}$

A.3. Startup Trajectory Generation

In this Appendix, the details for the computation of the startup voltage reference trajectory from Subsection 4.2.1 is documented. The desired polynomial $w(t) = V_{\mathrm{o,ref}}(t)$ for the startup trajectory is designed for a system of relative grade $r = 3$ and hence has grade $p = 2r + 2 = 7$ (see Subsection 4.2.1). The output voltage shall be transitioned from $40\,\mathrm{V}$ to $70\,\mathrm{V}$ within $200\,\mathrm{ms}$. According to the Subsection, the start value for the trajectory must be evaluated either by simulation or test, here, it is evaluated by simulation. [Lun14, Ch. 7] requires the reference trajectory to be in equal condition as the control signal, which is commonly zero for the functions first r derivations. In the simulation, this condition is reached at infinity due to the converging capacitor charging curve. Hence, the simulations exit condition is set to $< 1\,\mathrm{V/s}$ yielding approx. $41.1\,\mathrm{V}$ in the simulation. The reference trajectory starting point is then rounded to $V_{\mathrm{o,ref}}(t_0) = 40\,\mathrm{V}$, the first three derivations in t_0 are set to $\mathrm{d}^i V_{\mathrm{o,ref}}(t_0)/\mathrm{d}t^i = 0\,\mathrm{V/s}^i\ \forall\, i \in \{1, 3\}$. For the end point t_e, the trajectory shall have reached the steady state target voltage, hence it is $V_{\mathrm{o,ref}}(t_\mathrm{e}) = 70\,\mathrm{V}$ and the first three derivatives vanish. Start- and end point time instances are set to $t_0 = 0\,\mathrm{ms}$ and $t_\mathrm{e} = 200\,\mathrm{ms}$, respectively.

With those eight boundary conditions a system of eight linear equations is set up to compute the trajectories eight unique coefficients by computer numeric software. The specific trajectory to steer the converter output voltage from $40\,\mathrm{V}$ to $70\,\mathrm{V}$ within $200\,\mathrm{ms}$ is

$$V_{\mathrm{o,ref}}(t) = -109375000t^7 + 76562500t^6 - 18375000t^5 + 1531250t^4, \qquad \text{(A.30)}$$

where the coefficients for $t^3 \ldots t^0$ vanish.

A.4. Extended Converter FHA Model – Equation Derivation

The converter gain map to compute the feed forward control law in Subsection 4.2.3 is computed from an enhanced converter FHA model. This model extends the standard FHA model from literature, e.g., [Hua10] by the dissipative losses R_1, R_2 and R_{Fe} and the transformer primary and secondary leakage inductances L_1 and L_2, respectively from the converter electrical equivalent circuit in Figure 4.1b. This yields for the impedance notation

$$\begin{aligned} M_{\mathrm{fha,ext}} &= \left| \frac{Z_{\mathrm{o}}}{Z_{\mathrm{tot}}} \right| \\ &= \left| \frac{Z_{\mathrm{o}}}{Z_1 + \frac{Z_{\mathrm{h}}(Z_2+Z_{\mathrm{o}})}{Z_{\mathrm{h}}+Z_2+Z_{\mathrm{o}}}} \right| \\ &= \left| \frac{Z_{\mathrm{o}}\left(Z_{\mathrm{h}}+Z_2+Z_{\mathrm{o}}\right)}{Z_1\left(Z_{\mathrm{h}}+Z_2+Z_{\mathrm{o}}\right)+Z_{\mathrm{h}}\left(Z_2+Z_{\mathrm{o}}\right)} \right|. \end{aligned} \tag{A.31}$$

And by inserting the converter models electrical parameters

$$\begin{aligned} M_{\mathrm{fha,ext}} = \Bigg| & \frac{R_{\mathrm{e}}\left(n^2R_2+\mathrm{j}\omega n^2L_2-\frac{\omega^2R_{\mathrm{Fe}}L_{\mathrm{M}}^2-\mathrm{j}\omega R_{\mathrm{Fe}}^2L_{\mathrm{M}}}{R_{\mathrm{Fe}}^2+\omega^2L_{\mathrm{M}}^2}+R_{\mathrm{e}}\right)}{\left(R_1+\mathrm{j}\left(\omega L_{1\mathrm{tot}}-\frac{1}{\omega C_{\mathrm{r}}}\right)\right)\left(n^2R_2+\mathrm{j}\omega n^2L_2-\frac{\omega^2R_{\mathrm{Fe}}L_{\mathrm{M}}^2-\mathrm{j}\omega R_{\mathrm{Fe}}^2L_{\mathrm{M}}}{R_{\mathrm{Fe}}^2+\omega^2L_{\mathrm{M}}^2}+R_{\mathrm{e}}\right)\dots} \\ & \frac{}{\dots-\frac{\omega^2R_{\mathrm{Fe}}L_{\mathrm{M}}^2-\mathrm{j}\omega R_{\mathrm{Fe}}^2L_{\mathrm{M}}}{R_{\mathrm{Fe}}^2+\omega^2L_{\mathrm{M}}^2}\left(n^2R_2+\mathrm{j}\omega n^2L_2+R_{\mathrm{e}}\right)}\Bigg| \\ = & \left|\frac{N}{D}\right|. \end{aligned} \tag{A.32}$$

Where N is the complex numerator polynomial of the variable f_{n}

$$\begin{aligned} N = & R_{\mathrm{Fe}}^2R_{\mathrm{e}}\left(n^2R_2+R_{\mathrm{e}}\right)+\omega^2\frac{L_{1\mathrm{tot}}C_{\mathrm{r}}}{L_{1\mathrm{tot}}C_{\mathrm{r}}}L_{\mathrm{M}}^2R_{\mathrm{e}}\left(n^2R_2-R_{\mathrm{Fe}}+R_{\mathrm{e}}\right) \\ & +\mathrm{j}\omega\sqrt{\frac{L_{1\mathrm{tot}}C_{\mathrm{r}}}{L_{1\mathrm{tot}}C_{\mathrm{r}}}}R_{\mathrm{e}}\left(R_{\mathrm{Fe}}^2\left(L_{\mathrm{M}}+n^2L_2\right)+\omega^2L_{\mathrm{M}}^2n^2L_2\right) \end{aligned}$$

$$
\begin{aligned}
=&R_{\mathrm{Fe}}^2 R_{\mathrm{e}} \left(n^2 R_2 + R_{\mathrm{e}}\right) \\
&+ f_{\mathrm{n}}^2 \frac{1}{L_{1\mathrm{tot}} C_{\mathrm{r}}} L_{\mathrm{M}}^2 R_{\mathrm{e}} \left(n^2 R_2 - R_{\mathrm{Fe}} + R_{\mathrm{e}}\right) \\
&+ \mathrm{j} f_{\mathrm{n}} \frac{1}{\sqrt{L_{1\mathrm{tot}} C_{\mathrm{r}}}} R_{\mathrm{e}} R_{\mathrm{Fe}}^2 \left(L_{\mathrm{M}} + n^2 L_2\right) \\
&+ \mathrm{j} f_{\mathrm{n}}^3 \frac{1}{L_{1\mathrm{tot}} C_{\mathrm{r}}} \frac{1}{\sqrt{L_{1\mathrm{tot}} C_{\mathrm{r}}}} L_{\mathrm{M}}^2 n^2 L_2,
\end{aligned}
\tag{A.33}
$$

that yields the numerator coefficients

$$
\begin{aligned}
A_0^{\mathrm{N}} =& R_{\mathrm{Fe}}^2 R_{\mathrm{e}} \left(n^2 R_2 + R_{\mathrm{e}}\right) \\
A_2^{\mathrm{N}} =& \frac{1}{L_{1\mathrm{tot}} C_{\mathrm{r}}} L_{\mathrm{M}}^2 R_{\mathrm{e}} \left(n^2 R_2 - R_{\mathrm{Fe}} + R_{\mathrm{e}}\right) \\
B_1^{\mathrm{N}} =& \frac{1}{\sqrt{L_{1\mathrm{tot}} C_{\mathrm{r}}}} R_{\mathrm{e}} R_{\mathrm{Fe}}^2 \left(L_{\mathrm{M}} + n^2 L_2\right) \\
B_3^{\mathrm{N}} =& \frac{1}{L_{1\mathrm{tot}} C_{\mathrm{r}}} \frac{1}{\sqrt{L_{1\mathrm{tot}} C_{\mathrm{r}}}} L_{\mathrm{M}}^2 n^2 L_2,
\end{aligned}
$$

where $A_i^{\mathrm{N}} \in \mathbb{R}$ are the numerator real and $B_i^{\mathrm{N}} \in \mathbb{R}$ the imaginary coefficients. Analog, the denominator polynomial is computed to

$$
\begin{aligned}
D = &\left(2\pi f_{\mathrm{sw}} R_1 {}^{1}\!/_{2\pi f_{\mathrm{r}}} \sqrt{\frac{C_{\mathrm{r}}}{L_{1\mathrm{tot}}}} + \mathrm{j}\left(f_{\mathrm{n}}^2 - 1\right)\right) \\
&\left(R_{\mathrm{Fe}}^2 \left(n^2 R_2 + R_{\mathrm{e}}\right) + \left(2\pi f_{\mathrm{sw}}\right)^2 \frac{\left({}^{1}\!/_{2\pi f_{\mathrm{r}}}\right)^2}{L_{1\mathrm{tot}} C_{\mathrm{r}}} L_{\mathrm{M}}^2 \left(n^2 R_2 - R_{\mathrm{Fe}} + R_{\mathrm{e}}\right)\right. \\
&\left. + \mathrm{j} 2\pi f_{\mathrm{sw}} \frac{{}^{1}\!/_{2\pi f_{\mathrm{r}}}}{\sqrt{L_{1\mathrm{tot}} C_{\mathrm{r}}}} \left(R_{\mathrm{Fe}}^2 \left(L_{\mathrm{M}} + n^2 L_2\right) + \left(2\pi f_{\mathrm{sw}}\right)^2 \frac{\left({}^{1}\!/_{2\pi f_{\mathrm{r}}}\right)^2}{L_{1\mathrm{tot}} C_{\mathrm{r}}} L_{\mathrm{M}}^2 n^2 L_2\right)\right) \\
&- L_{\mathrm{M}} R_{\mathrm{Fe}} \left(\left(2\pi f_{\mathrm{sw}}\right)^3 \frac{\left({}^{1}\!/_{2\pi f_{\mathrm{r}}}\right)^2}{L_{1\mathrm{tot}}} \frac{{}^{1}\!/_{2\pi f_{\mathrm{r}}}}{\sqrt{L_{1\mathrm{tot}} C_{\mathrm{r}}}} \left(L_{\mathrm{M}} n^2 R_2 + n^2 L_2 R_{\mathrm{Fe}} + L_{\mathrm{M}} R_{\mathrm{e}}\right)\right. \\
&\left. - \mathrm{j}\left(2\pi f_{\mathrm{sw}}\right)^2 \frac{\left({}^{1}\!/_{2\pi f_{\mathrm{r}}}\right)^2}{L_{1\mathrm{tot}}} \left(R_{\mathrm{Fe}} n^2 R_2 + R_{\mathrm{Fe}} R_{\mathrm{e}} - \left(2\pi f_{\mathrm{sw}}\right)^2 \frac{\left({}^{1}\!/_{2\pi f_{\mathrm{r}}}\right)^2}{L_{1\mathrm{tot}} C_{\mathrm{r}}} L_{\mathrm{M}} n^2 L_2\right)\right)
\end{aligned}
$$

$$
\begin{aligned}
&= f_\mathrm{n}\sqrt{\frac{C_\mathrm{r}}{L_\mathrm{1tot}}}R_1R_\mathrm{Fe}^2\left(n^2R_2+R_\mathrm{e}\right)\\
&f_\mathrm{n}^3\frac{1}{\sqrt{L_\mathrm{1tot}C_\mathrm{r}}}\frac{L_\mathrm{M}^2}{L_\mathrm{1tot}}R_1\left(n^2R_2-R_\mathrm{Fe}+R_\mathrm{e}\right)\\
&+\mathrm{j}f_\mathrm{n}^2\frac{1}{L_\mathrm{1tot}}R_1R_\mathrm{Fe}^2\left(L_\mathrm{M}+n^2L_2\right)\\
&+\mathrm{j}f_\mathrm{n}^4n^2\frac{L_\mathrm{M}^2L_2}{L_\mathrm{1tot}^2C_\mathrm{r}}R_1\\
&+\mathrm{j}f_\mathrm{n}^2R_\mathrm{Fe}^2\left(n^2R_2+R_\mathrm{e}\right)\\
&-\mathrm{j}R_\mathrm{Fe}^2\left(n^2R_2+R_\mathrm{e}\right)\\
&+\mathrm{j}f_\mathrm{n}^4\frac{L_\mathrm{M}^2}{L_\mathrm{1tot}C_\mathrm{r}}\left(n^2R_2-R_\mathrm{Fe}+R_\mathrm{e}\right)\\
&-\mathrm{j}f_\mathrm{n}^2\frac{L_\mathrm{M}^2}{L_\mathrm{1tot}C_\mathrm{r}}\left(n^2R_2-R_\mathrm{Fe}+R_\mathrm{e}\right)\\
&-f_\mathrm{n}^3\frac{1}{\sqrt{L_\mathrm{1tot}C_\mathrm{r}}}R_\mathrm{Fe}^2\left(L_\mathrm{M}+n^2L_2\right)\\
&+f_\mathrm{n}\frac{1}{\sqrt{L_\mathrm{1tot}C_\mathrm{r}}}R_\mathrm{Fe}^2\left(L_\mathrm{M}+n^2L_2\right)\\
&+\mathrm{j}f_\mathrm{n}^4n^2\frac{L_\mathrm{M}^2L_2}{L_\mathrm{1tot}C_\mathrm{r}}\\
&-\mathrm{j}f_\mathrm{n}^2n^2\frac{L_\mathrm{M}^2L_2}{L_\mathrm{1tot}C_\mathrm{r}}\\
&-f_\mathrm{n}^3\frac{L_\mathrm{M}}{L_\mathrm{1tot}}\frac{1}{\sqrt{L_\mathrm{1tot}C_\mathrm{r}}}R_\mathrm{Fe}\left(L_\mathrm{M}n^2R_2+n^2L_2R_\mathrm{Fe}+L_\mathrm{M}R_\mathrm{e}\right)\\
&+\mathrm{j}f_\mathrm{n}^2\frac{L_\mathrm{M}}{L_\mathrm{1tot}}R_\mathrm{Fe}\left(n^2R_\mathrm{Fe}R_2+R_\mathrm{Fe}R_\mathrm{e}\right)\\
&-\mathrm{j}f_\mathrm{n}^4n^2\frac{L_\mathrm{M}^3L_2}{L_\mathrm{1tot}^2C_\mathrm{r}}R_\mathrm{Fe},
\end{aligned}
\tag{A.34}
$$

and its coefficients are

$$A_1^{\mathrm{D}} = \sqrt{\frac{C_\mathrm{r}}{L_{1\mathrm{tot}}}} R_1 R_{\mathrm{Fe}}^2 \left(n^2 R_2 + R_\mathrm{e}\right) + \frac{1}{\sqrt{L_{1\mathrm{tot}} C_\mathrm{r}}} R_{\mathrm{Fe}}^2 \left(L_\mathrm{M} + n^2 L_2\right)$$

$$\begin{aligned} A_3^{\mathrm{D}} = & \frac{1}{\sqrt{L_{1\mathrm{tot}} C_\mathrm{r}}} \left(\frac{L_\mathrm{M}^2}{L_{1\mathrm{tot}}} \left(R_1 \left(n^2 R_2 + R_\mathrm{e} - R_{\mathrm{Fe}}\right) - R_{\mathrm{Fe}} \left(n^2 R_2 + R_\mathrm{e}\right)\right) \right. \\ & \left. - R_{\mathrm{Fe}}^2 \left(L_\mathrm{M} \left(n^2 \frac{L_2}{L_{1\mathrm{tot}}} + 1 \right) + n^2 L_2 \right) \right) \end{aligned}$$

$$B_0^{\mathrm{D}} = - R_{\mathrm{Fe}}^2 \left(n^2 R_2 + R_\mathrm{e}\right)$$

$$\begin{aligned} B_2^{\mathrm{D}} = & \frac{1}{L_{1\mathrm{tot}}} \left(R_{\mathrm{Fe}}^2 \left(\left(L_{1\mathrm{tot}} L_\mathrm{M}\right) \left(n^2 R_2 + R_\mathrm{e}\right) + R_1 \left(L_\mathrm{M} + n^2 L_2\right)\right) \right. \\ & \left. - \frac{L_\mathrm{M}^2}{C_\mathrm{r}} \left(n^2 \left(R_2 + L_2\right) + R_\mathrm{e} - R_{\mathrm{Fe}} \right) \right) \end{aligned}$$

$$B_4^{\mathrm{D}} = \frac{L_\mathrm{M}^2}{L_{1\mathrm{tot}} C_\mathrm{r}} \left(n^2 \left(\frac{L_2}{L_{1\mathrm{tot}}} R_1 R_2 + L_2 - \frac{L_\mathrm{M} L_2}{L_{1\mathrm{tot}}} R_{\mathrm{Fe}} \right) + R_\mathrm{e} - R_{\mathrm{Fe}} \right).$$

A.5. Converter Design Parametrization and Scaled Model Parametrization

Table A.2 summarizes the LLC converters key parametrization. The dependent parameter in the tables lower part is computed with the input of the converters design parameters and the choosen components for the pertaining example. The *Large-Scale* column gives a parametrization example i.e., for a modular converter for the mobile machine tethering example from Section 3.4. The transformer parametrization is computed for a transformer design with two sets of core material of type *Epcos UU93/152/30* with core material *N27*. Subsequently, the non-transformer parameters (f_{r1}, L_n, C_r) are computed. The *Small-Scale* converter is derived from the mobile machine converter with voltage and power reduced to a scale, where experiments are less hazardous due to lower voltage and power dissipation by easy means. It is wholly expected, that general statements regarding the system behavior can be made with the scaled prototype. Here, all voltage values are scaled by $1/10$ and power values by $1/1000$. Deviations to the scaling factors result from corrections made to the scaling as results during the prototype design and initial test operation. In the *Small-Scale* column,

Table A.2.: Model parametrization for the system analysis

Component	*Value*	
	Large Scale	*Small Scale*
Design Parameter		
Nominal Power	60 kW	30 W
V_{in}	550 V	55 V
V_{o}	900 V	70 V
f_{r}	48 kHz	59.3 kHz
L_{r}	330 µH	470 µH
C_{o}	47 µF	3.3 µF
Dependent Parameter		
L_1	0.95 µH	9.8 µH
$L_{1\mathrm{tot}} = L_1 + L_{\mathrm{r}}$	331 µH	480 µH
R_1	0.53 mΩ	23 mΩ
L_{M}	475 µH	2.1 mH
R_{Fe}	9.4 kΩ	4.3 kΩ
L_2	4.98 µH	22 µH
R_2	2.3 mΩ	82 mΩ
Transformer Turns Ratio	$7/16$	$14/21$
f_{r1}	30 kHz	25.5 kHz
L_{n}	1.4	4.4
C_{r}	33 nF	15 nF

dependent transformer parameters are documented from prototype measurement and computation, where measurement was not achievable.

Table B.1.: Key parameter for the system simulation configuration

Setting	*Symbol*	*Value*
Simulink solver		*Backward Euler* (discrete)
Solver type		Fixed step size
Circuit sampling rate	$T_{\mathrm{s,M}}$	$0.025\,\mu\mathrm{s}$
Controller sampling rate	$T_{\mathrm{s,C}}$	$100\,\mu\mathrm{s}$
Recorded data sampling rate	$T_{\mathrm{s,R}}$	$100\,\mu\mathrm{s}$
Voltage source resistance	R_{i}	$0.1\,\Omega$
Inverter dead time	t_{d}	$400\,\mathrm{ns}$
Simulated IGBTs	$D_1, \ldots, D_8$	*Vishay: ESH2PD*
Simulated diodes	$S_1, \ldots, S_4$	*STMicroelectronics: STGB6NC60HD*
Simulated core material	T_1	*Epcos: RM10, N87*

B. Converter Concept Validation and Evaluation

B.1. Simulation Model Setup and Parametrization

The simulative evaluations for this work are performed with simulation models under *The Mathworks, Inc.*s computer numeric software package *Matlab/Simulink*, a tool for numeric time domain simulations of dynamic systems (further referenced as *Simulink*). Within the models, the LLC converters power electronic circuits are physically modeled with the *SimScape* toolbox – a *The Mathworks, Inc.* provided toolbox for simulation of physical domains on *Simulink*. The key parametrization of the simulation models is summed up in Table B.1, in Figure B.1, the model structure is depicted.
The model overview with a controller and a circuit subsystem is given in Subfigure B.1a. The electronic circuit is operated at a sampling rate of $T_{\mathrm{s,M}} = 0.025\,\mu\mathrm{s}$, while

Table B.2.: Voltage and current sensors, used on the prototype

Device	*Manufacturer*	*Type*	*Nominal Value*	*Measuring Range*
Voltage sensor	*LEM*	*LV 25-P*	84.5 V	−700 – 700 V
Current sensor	*Sensitec*	*CMS2005*	±5 A	−20 – 20 A

the controller domain operates at $T_{\mathrm{s,C}} = 100\,\mu\mathrm{s}$. Data, that is exchanged between both domains is routed through rate transmission blocks, as given in the figure.

The controller and the electronic circuit (exemplarily single module converter) subdomains are given in Subfigures B.1b and B.1c, respectively.
The converters physical model is equal to the concepts given in this publication, modeling details to key components are given in the Table. The power supply is modeled as a DC voltage source with an inner resistor – located left in the model. The variable load is modeled as a resistor with a tunable counter DC source to control the current flow – and hence the power dissipation – through the load resistor. The load-source is controlled by the load reference profile. The measurement points for the data recording, utilized for the figures in the evaluation chapter, are documented in the circuit.
The controller subsystem in the last subfigure consists of the controller structure, introduced in Subsection 4.2.2. To the subfigure's left, the voltage reference generation block is situated. It also contains the computation of AC values from its according DC measurements. AC and DC outputs of the reference generator block are marked by a corresponding bracketed tag on the output ports. To the subfigures right a block is located, where the pulse patterns for the IGBT operation is computed from the converter switching frequency f_{sw}. The pulse pattern is generated with a dead time of $t_{\mathrm{d}} = 400\,\mathrm{ns}$.

B.2. Prototype Design Documentation

The LLC converter circuit concept from Section 3.2 is prototypically implemented in the low voltage domain for basic proof of concept experiments. For the circuit realization, the parametrization and components modeled for the simulation models are used (see Appendix B.1 and there, especially Table B.1).

The prototype is driven by a variable frequency, 50 %-duty cycle PWM signal in the desired converter operating frequency f_{sw}. For this driver signal, a galvanically isolated input port is provided to protect the connected source from potential damage

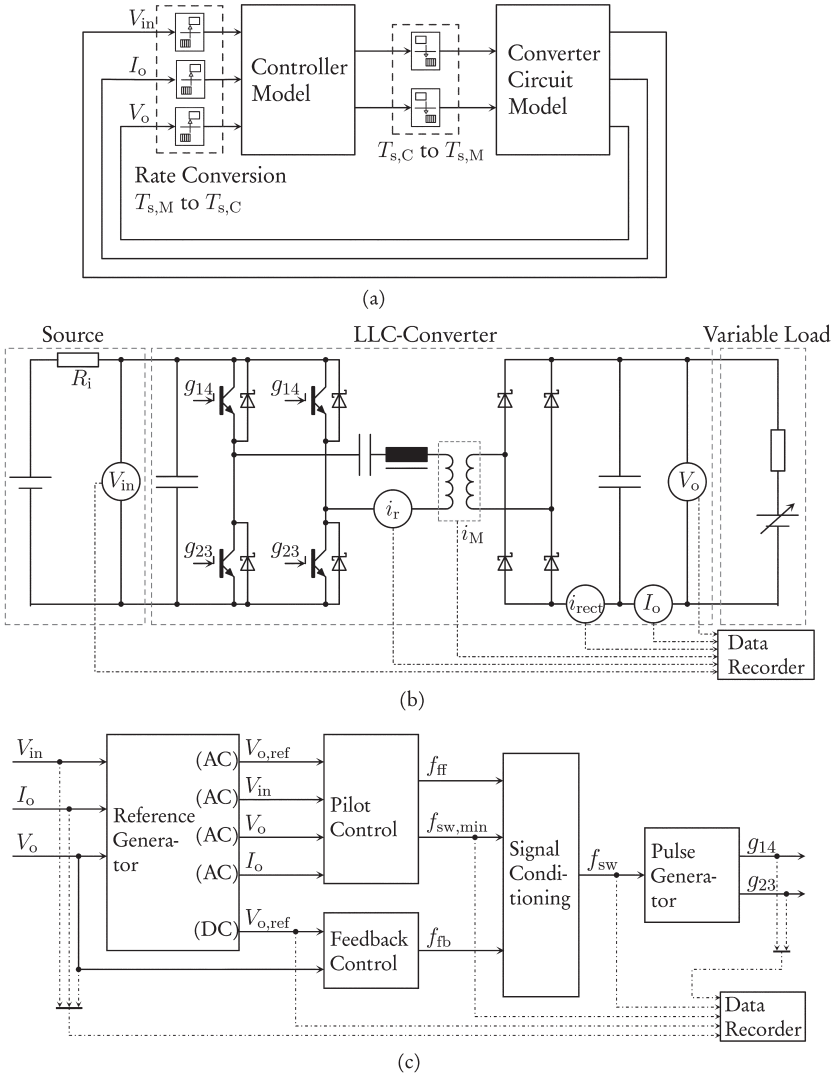


Figure B.1.: Simulation model architecture: Model overview (a) with sampling time domains, physical LLC Converter circuit (b) and controller model (c) with data recording tappings.

due to electrical failures of the prototype and as part of the galvanic separation concept from Figure 3.7 in a modular converter setup. On the prototype Printed Circuit Boards (PCB), the driver signal is electrically inverted for the H-bridges second arm ($IGBT_3, IGBT_4$) and amplified by an of the shelf IGBT driver Integrated Circuit (IC) for IGBT actuation.
To provide measurement feedback to the controller device, the converter circuit on the prototype is extended by voltage sensors for the DC input and output voltages V_{in} and V_{o}, respectively and a current sensor for the DC output current I_{o}. The sensor types and key parameters are given in Table B.2. While the nominal value for the voltage sensor, given in the table is fitted to the application's needs; the current sensor has a fixed nominal value that cannot be adjusted. Both sensors provide the required galvanic isolation from the power circuit to the control computer. Also, the sensor power supplies – one for the primary side and one for the secondary side sensors – are galvanically isolated to meet the demands of the concept from Figure 3.7.
The prototypes are mounted in plastic housings and can be connected to modular converters in accordance with the modular DC/DC converter concept from Section 3.1.

B.3. Hardware in the Loop Test Setup

Figure B.2 sketches the component overview and wiring diagram for the HIL setup, that is used to execute this publications experiments on the single module converter example. The prototypes input DC voltage supply is generated by the *DC Supply* in the top left, which is realized by a galvanically isolated laboratory power supply unit, it is manually tuned to $V_{\mathrm{in}} = 55\,\mathrm{V}$. A second galvanically isolated laboratory supply unit *Aux. Supply* supplies the rapid prototyping computer of type *dSpace AutoBox*, the *Control Panel* is used to start and stop the converters power transmission. The *Prototypical Converter* is one module of the LLC converter, as described in section 3.2, the prototype setup is documented in Appendix B.2. The digital control signals are transmitted from the *AutoBox* to the converter and analog sensor signals are routed vice versa. The sensor signals are read in by the *AutoBox*s Analog to Digital Converter (ADC) channels. The converter load is realized by an electronic load with two load channels, for each channel one load resistor value is predefined: One for the full load case, the second for the half load case. During the benchmark test (Subsection 4.2.6), the full- and half-load pattern is emulated by manually switching between the two channels.
For the modular DC/DC converter experiments, additional converter modules are connected according to the desired input-output topology to the *DC Supply*, the

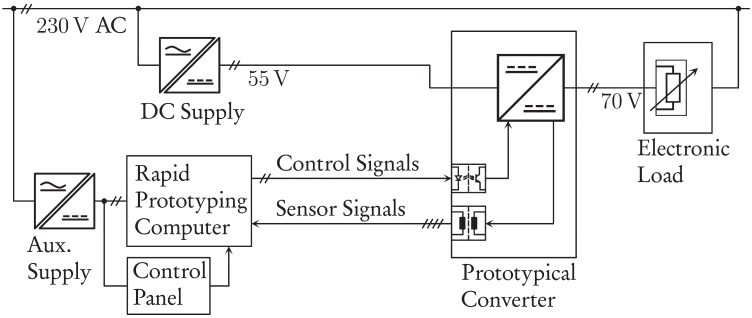


Figure B.2.: Component overview and wiring diagram of the HIL setup with one converter module for the experiments within this publication.

existing module and the *Electronic Load*. For the additional modules *Control Signals* and *Sensor Signals* from and to the *AutoBox*, additional *AutoBox* I/O channels are utilized.

For the control software on the *AutoBox*, the controller part from the simulation model in Appendix B.1 is automatically translated to executable source code, compiled and uploaded to the *AutoBox*, where it is executed. Therefore, *dSpace* provides a block set to integrate *AutoBox* in- and outputs in the *Simulink* model for once and second a toolchain for the required steps to run the model on the *AutoBox*. During the software build, the controller cycle time is automatically set to the *Simulink* solvers step size in the root simulation model – in this case, 100 µs.

The data acquisition for post experimental evaluation is realized by an ethernet-connected PC with *dSpaces* software package *ControlDesk*. With this tool, software signals from the control models can be observed on a dashboard and be recorded during the experiment for ether evaluation within the software or exporting for post processing with any other software. The recording sampling time during the experiments is set to 100 µs for all measurements.

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Kurzfassung

Die Bemühungen zur Dekarbonisierung führen zur Elektrifizierung, nicht nur bei Straßenfahrzeugen, sondern auch bei mobilen Arbeitsmaschinen. Neben Batterien werden diese durch Schleppleitungssysteme mit AC-Niederspannung elektrifiziert. Solche Systeme werden z.B. bei Untertage-Radladern mit kurzen Leitungen und geringer Leistung eingesetzt. Um Schleppleitungen in weitere Märkte wie Landmaschinen auszuweiten, wird eine HVDC-Anbindung vorgeschlagen, die durch dünnere, leichtere Leitungen höhere Maschinenleistung und Übertragungslänge erlaubt. Die hohe Leitungsspannung wird durch in Reihe geschalteten DC/DC-Wandler aufgeteilt und gewandelt. Geringe Sperrspannung ermöglicht den Einsatz schnell schaltender Halbleiter, um Wandler-Gewicht und -Volumen zu reduzieren. Das modulare Konzept lässt sich flexible an verschiedene Anforderungen anpassen. Da vergleichbare Konzepte für Offshore-Windparks existieren, wird seine Anwendbarkeit für diese diskutiert. Für die Module wird ein Vollbrücken-LLC Resonanzwandler vorgestellt. Ein switched LTI Modell wird abgeleitet und die Stabilität durch eine Common Quadratic Lyapunov Function (CQLF) nachgewiesen. Die Spannungsregelung enthält eine Softstart Methode und Regelung über alle Module. Die Konzepte werden simulativ und prototypisch validiert.

Abstract

Efforts in decarbonization lead to electrification, not only for road vehicles but also in the sector of mobile machines. Aside from batteries, those machines are electrified by tethering systems, nowadays featuring an AC low voltage system. Those systems are applied, e.g., to underground load haul dumpers with short tethering lines and low machine power. To expand tethering to further markets as agricultural machinery, this work proposes an HVDC tethering system allowing higher machine power and transmission length due to thinner, lighter tethering lines. The HVDC voltage is converted by distribution over a number of series connected DC/DC converters. Less blocking voltage on the semiconductors allows faster switching technology to reduce the converters' weight and volume. The concepts modularity allows for flexible adaption on various application scenarios. Since comparable concepts exist for offshore wind farms connectivity, its applicability for this is discussed. A full bridge inverter/rectifier LLC resonance DC/DC converter is presented for the modules. A switched LTI converter model is developed and a Common Quadratic Lyapunov Function (CQLF) is computed for prove of stability. The converter control features soft startup and voltage control over all modules. The concepts are validated by simulation and on a scaled prototype.